Curriculum Vitæ

Marco D. Santambrogio

Contents

1 Personal Data

1.1 General data

Name Marco Domenico

Surname Santambrogio

Date of birth November 04, 1977

Place of birth Monza (MI) - Italy

Citizenship Italian

Marital status Married

1.2 Office address

Computer Science and Artificial Intelligence Laboratory
Massachusetts Institute of Technology
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Research groups:
DRESD: http://www.dresd.org
CARBON: http://groups.csail.mit.edu/carbon/

1.3 Academic positions and affiliations

- Academic positions

Since 11/2009 Assistant Professor at the Dipartimento di Elettronica ed Informazione of Politecnico di Milano (Milano, Italy).

Since 12/2009 Adjunct Professor in the College of Engineering of University of Illinois at Chicago (Chicago, Illinois, USA).

Since - 03/2010 Research Affiliate at Massachusetts Institute of Technology - Computer Science and Artificial Intelligence Laboratory (Cambridge, MA - USA).

02/2010 - 02/2009 Postdoc Fellow (research : Self-Aware Computing Systems.) at Massachusetts Institute of Technology - Computer Science and Artificial Intelligence Laboratory (Cambridge, MA - USA).

07/2008 - 10/2009 Research Assistant (research program: Metodologie di progetto di sistemi informatci hardware e software. (Design methodologies for hardware and software IT systems.)) at the Dipartimento di Elettronica ed Informazione of Politecnico di Milano (Milano, Italy).

03/2008-07/2008 Research Assistant (research program: Analisi e definizione di possibili scenari applicativi di nuovi sistemi riconfigurabili. (Analysis and definition of applicative scenarios for novel reconfigurable technologies.)) at the Dipartimento di Elettronica ed Informazione of Politecnico di Milano (Milano, Italy).

03/2005-07/2008 PhD Student in the Computer Engineering and Automation program at the Dipartimento di Elettronica ed Informazione of Politecnico di Milano (Milano, Italy).

11/2004-03/2005 Research Assistant (research program: Definizione di un flusso di design per sistemi riconfigurabili basati su FPGA della Xilinx. (Definition of a novel design flow for Xilinx FPGA-based reconfigurable systems.)) at the Dipartimento di Elettronica ed Informazione of Politecnico di Milano (Milano, Italy).

- Affiliations

Since 2008 Member of the IEEE Computer Society (CS)

Since 2008 Member of the IEEE Circuits and Systems Society (CAS)

Since 2005 Member of the Institute of Electrical and Electronic Engineers (IEEE)

Since 2008 Member of the Association for Computing Machinery (ACM)

Since 2005 Member of the Italian Association of Operations Research (AIRO)

Since 2008 Member of HipEAC, European Network of Excellence on High Performance and Embedded Architecture and Compilation

Since 2008 Member of HiPEAC Reconfigurable Computing Cluster

Since 2009 Member of the Italian Scientists and Scholars of North America Foundation (ISSNAF)

1.4 Education

February 2008 PhD in Information Engineering
DIPARTIMENTO DI ELETTRONICA ED INFORMAZIONE, POLITECNICO DI MILANO
PhD Thesis: *Hardware/Software codesign methodologies for dynamically reconfigurable systems.*
Advisor: Prof. D. Sciuto. Tutor: Prof. F. Ferrandi

June 2004 Master of Science in Computer Science
UNIVERSITY OF ILLINOIS AT CHICAGO, CHICAGO, ILLINOIS, USA
Master Thesis: *Dynamic Reconfigurability in Embedded System Design. A Model for the Dynamic Reconfiguration.*
Advisor: Prof. John Lillis.

April 2004 Laurea (MSc italian equivalent) in Computer Engineering
POLITECNICO DI MILANO
Thesis: *A Methodology for Dynamic Reconfigurability in Embedded System Design.*
Advisor: Prof. D. Sciuto.

July 1996 Diploma di Maturita' Scientifica
High-school diploma specializing in scientific studies
LICEO SCIENTIFICO G. PEANO (Cinisello Balsamo).

1.5 Visiting periods

- Postdoc Fellow, Massachusetts Institute of Technology, February 2009 - now
- Visiting researcher, Heinz Nixdorf Institute, January 2009
- Invited researcher, Northwestern University, April - May 2007
- Invited researcher, Northwestern University, February - June 2006
- Visiting researcher, Heinz Nixdorf Institute, January 2006
- MSc Student, University of Illinois at Chicago, 2002

1.6 Other information

Since 03/2009 Member of the MIT Postdoctoral Advisory Council.

Since 12/2009 Member of the National Postdoctoral Association (NAP).

01/2009 Co-founder and president of the iDRESD Association.

07/2005 - 12/2006 Head of the ICT area and member of the managing board of ISF-MI Association.

July 2005 Co-founder of Engineer Without Border Milano (Ingegneria Senza Frontiere ISF-MI).

01/2001- 04/2001 Head of the IT area, for Caritas Ambrosiana and CeLIM, of two humanitarian missions in Kosovo (Jacova e Pristina)

02/2000 - 12/2000 Civil service at CeLIM NGO.

2 Scientific Activities

2.1 Research interests

2.1.1 Self-adaptable and autonomic systems

Self-adaptive computer systems are capable of adapting their behaviour and resources thousands of times a second based on changing environmental conditions and demands [**G.6**]. This allows them to automatically find the best way to accomplish a given goal with the resources at hand [**E.26**]. This capability would benefit the full range of computer systems, from embedded devices to servers to supercomputers. Some of the main challenges in realizing such a vision are: to add auto-adaptability capabilities to organic devices, to implement distributed self-training algorithms over such architectures, and to specify and formulate application solutions using such a computing paradigm [**E.25**]. Within this context, a self-adaptive and autonomic computing system is no longer view as a static bunch of hardware components with a passive set of applications running on top of an operating system used to properly coordinate the underling hardware architecture. It becomes an active system where either the hardware, the applications and the operating system have to be seen as an unique entity that have to be able to autonomously adapt itself to achieve the best performance[1]. The advantages of such complex, adaptable, highly-parallel, evolvable heterogeneous multicore systems could be applied in various fields such as: biomedical implants (e.g. self-evolvable implants that will adapt their computation to the characteristics of the environment where they've been implanted), telecommunications (e.g. adaptive intelligent routers and cognitive networks that are looking for high-performance, adaptable mobile devices), Data Center on Chip (spatially organized modular applications architecture taking lessons from internet-like distributed, fault-tolerant, applications), high accuracy speech processing, intelligent transducers at bio-electronic interfaces, etc.

2.1.2 Hardware/Software codesign methodologies for dynamically reconfigurable systems

In this research [**E.1**] I introduce a new design framework which amends this lack. Therefore aim of this research is to define a methodology and design flow, named *earendil* [**E.8, D.14, D.9, E.19**], for reconfigurable embedded systems which aims at defining a specification-to-bistream and autonomous design flow based on, where possible, standard tools. The idea behind the proposed methodology [**C.1, E.1, E.2, D.2**] is based on the assumption that it is desirable to implement a flow that can output a set of configuration bitstreams used to configure and, if necessary, partially reconfigure a standard FPGA to realize the desired system. One of the main strengths of the proposed methodology is its low-level architectural independence. In fact it has been developed using both the Caronte [**E.1, F.2, F.3, E.4**] and the YaRA (Yet another Reconfigurable Architecture) architecture [**G.3**], but it can be easily adapted to different architectural and SoC solutions, i.e. the RAPTOR2000 system. The earendil design flow consists mainly of three phases:

- The **High Level Reconfiguration** phase, which is the first step performed in the earendil flow. Its goal is to analyze the input specification in order to find a feasible representation, produced by a first partitioning (cores/functionalities identification) phase, that can be used to perform the hardware/software codesign. In the currently implemented framework, cores are identified by extraction of isomorphic templates used to generate a set of feasible covers of the original specification. Finally, the computed cover is placed and scheduled onto the given device.

- The **Validation** phase. Aim of the *validation* phase is to drive the refinement cycle of the system design [**D.6**]. Using the information provided by this phase, it is possible to modify the decisions taken in the first part of the flow to improve the development process.

- The last step that has to be performed is the (Low Level Reconfiguration) phase. Goal of this step is the definition of an automatic generation of the low-level implementation of the final solution that has to be physically deployed on the target device and that realizes the original specification [**E.4, D.8, D.29, D.33, D.24, E.21**].

[1] Where performance can have different meaning according to a specific scenario. It is possible to have a system trying to maximize the overall completion time of a set of applications, and, under different constraints, having the same system running trying to minimize its power consumption.

2.1.3 Placement, partitioning and scheduling of task graphs on partially dynamically reconfigurable architectures

Goal of this research is the creation of a complete theory and workflow [**A.3, E.1, D.21, D.27**] to help the designer in the specification and management of reconfigurable systems. The provided support is related to the definition of area constraints for tasks [**E.15, G.5**], reconfiguration specific constraints, like reconfiguration time [**A.3, D.7, D.25**], manipulation of the input specification, placement assignment [**C.3, D.12, D.18, D.27**] to each core defining the input specification, partitioning the input specification [**D.3**] and so forth. The aim is to develop an automated tool capable of helping the designer and prepare the input specification for low level design phases. Moreover, self, partial and dynamical reconfiguration, in both its mono-dimensional (1D) and bi-dimensional (2D) paradigms, gives the possibility of enhancing the flexibility of a reconfigurable system. As we have seen, it is a powerful approach but, at the same time, causes a significant increase in the complexity of system creation and management. Therefore, one of the goals of these studies is to support the designer in creating and managing a reconfigurable system, starting from the higher description of the desired system, to the identification, once the target architecture has been defined, of the online cores placement and in the core relocation support [**A.2, D.10, E.13**], combining the online cores placement with the runtime bitstreams relocation [**A.2**]to implement a complete solution that can be used in conjunction with the runtime self reconfiguration.

2.1.4 Scheduling problems with uncertainty conditions

This work starts from the classical resource constrained scheduling problem: a set of tasks has to be executed using a fixed and limited amount of resources. Each task is characterized by a duration (the time required to complete its execution). Precedence constraints ordered pairs of tasks prescribing that the latter must start only after the former has ended. Mapping constraints define the resource on which each task must be executed. Aim of this research was to introduce two extensions of the previously described framework: *multi-mode execution* and *conditional execution*. With Multi-mode execution, a task can be performed using different alternative resources, having different performances, i.e. execution time. Some tasks must be executed by a specific resource, others can be executed using different resources. While Conditional execution means that not all the tasks must be executed. the execution of a task is subject to the occurrence of an external event, which is unpredictable at the beginning of the schedule. Different event combinations provide different subsets of tasks to be performed, that means different scheduling problems to be solved. The main objective of this research was to minimize the overall execution time [**D.4**], independently from the events occurred, by applying Integer Linear Programming (ILP) techniques. Different applicative fields [**E.1**] have been taken into account to prove both the practical relevance of the problem considered and the generality of the proposed approach.

2.1.5 An operating system support runtime management for partially dynamically reconfigurable embedded systems

The increasing amount of programmable logic provided by modern FPGAs makes it possible to execute multiple hardware applications on the same device. This approach is reinforced by dynamic reconfiguration, which allows a single part of the device to be configured with a single hardware module. In this scenario, an operating system can be developed in order to determine where a module should be configured, and to provide an interface towards the final user in order to request a hardware application in a simplified way. The proposed solution is a complete operating system to manage on-demand module configuration on an FPGA while providing a set of high-level abstractions to user applications. The development of an operating system for reconfigurable devices makes the whole system more flexible [**D.1**], and increases the level of abstractions for the final user [**D.29**]. The proposed methodology [**C.1, D.29**] focuses on the extension of a well-known and portable kernel such as GNU/Linux, in order to introduce a support for dynamic reconfiguration and to simplify the interface between the user application and the reconfigurable hardware [**E.16**]. Each software application, also named *process*, can issue one or more system calls in order to require a specific functionality, which may be available either as a software library, or as a hardware IP-Core, or both. The operating system is in charge of choosing among the software or the hardware implementation according to different criteria, such as the amount of free area on the FPGA. The reconfiguration support in the operating system has been implemented by means of two kernel modules and a reconfiguration library [**D.29**]. Those three elements are part of a layered structure, in which software applications communicate with the kernel by means of

the functions of the reconfiguration library. Until now, the main contributions of this research can be summarized in the following two points: in an extensive and complete design flow for the self reconfiguration of SoC architectures via an extension of a standard operating system like GNU/Linux [**C.1, E.16**] and in the design of an Operating System solution able to support and manage the reconfiguration both in a SoC [**C.1, D.1, E.23**] or in Multi-FPGAs scenario [**D.13, D.29**].

2.1.6 Combining software Adaptive Computation and reconfigurable hardware techniques for exploring novel SoC design solutions

In existing approaches to codesign, the emphasis is placed on identifying computationally intensive tasks, also called kernels, and then maximizing performance by implementing most of these tasks on reconfigurable hardware. In this scenario, software primarily performs the control dominated tasks. The performance model of the reconfigurable hardware is mainly defined by the degree of parallelism available in a given task and the amount of reconfiguration and communication cost that will be incurred. The performance model for software execution is on the other hand static and does not become affected by external factors. The proposed methodology [**D.11, D.16**] aims to provide the necessary metrics [**E.9**] and evaluation tools to compare and choose the best implementation within a larger search space that we refer to as the gray area between hardware and software domains. We argue that with the innovations in both software optimization techniques as well as hardware technologies, the codesign task for reconfigurable SoCs will have to navigate a larger gray area than before. We propose to incorporate an effective software optimization technique, based on Adaptive Computing, and the emerging dynamic reconfiguration technology for hardware into one design framework [**D.16**] and explore the best of both worlds with a novel set of performance metrics and evaluation tools.

2.1.7 Computer architecture and multi-core heterogeneous systems

GPP-based reconfigurable processing elements. FPGAs can be used to create hardware/software platforms that keep their flexibility after deployment, allowing the development of complex *System-on-Chip* (SoC) and reducing the overall number of physical components, since many resources can be configured on request, replacing unused ones. In such a scenario, a larger number of complex components can be mapped at the same time into the same device [D.28]. An emerging design pattern is based on Multi Processing Element. This research focuses its attention on the definition of a Reconfigurable Processing Element based on a Harvard Architecture, called HARPE [**E.18**]. HARPE's architecture includes a MicroBlaze soft-processor in order to make HARPEs deployable also on devices not having processors on silicon die. In such a context, this work also introduces a novel approach for the management of processor data memory. The proposed approach allows the individual management of data and the dynamic update of the memory [**D.20**], thus making it possible to define Partially Dynamical Reconfigurable Multi Processing Element Systems, that consist of several master (e.g., soft-processors, hard-processors or HARPE cores) and slave components. Finally, the proposed methodology enables the possibility of creating a system in which both HARPEs and their memories (data and code) can be separately configured at run time with a partial configuration bitstream, in order to make the whole system more flexible with respect to changes occurring in the external environment. This situation will lead to the definition of an adaptable multi-processors reconfigurable architecture.

Design of dedicated CPU for regular expression matching. In many applications, string pattern matching is one of the most intensive task in terms of computation time and memory accesses. Network Intrusion Detection Systems and DNA Sequence Matching are two of those. Since software solutions are not able to satisfy the requirements in terms of performance, specialized hardware architectures are required. In [**C.2, D.17**] a complete framework for regular expression matching has been proposed. The proposed special-purpose processor, called ReCPU, is programmed using a regular expression programming language. The parallelism adopted in the design grants the possibility to achieve a throughput greater than one character per clock cycle requiring $O(n)$ memory space. The VHDL description of the proposed architecture is fully configurable and the design space exploration to find the optimal architecture based on area and performance cost-function has been presented in [**D.26**]. The reconfigurable version of ReCPU can be configured on programmable devices such as a FPGAs, with a set of ReCPUs, each one exploiting a single instance of the regular expression matching task on the given input string. These cores work in parallel on the same string analyzing different possible matching of the regular expression.

Since the system is able to exploit dynamic partial reconfigurations, it can adapt at run-time the number of cores configured on the device, therefore it is possible to parallelize the regular expression matching process with a multiple cores architecture drastically reducing the time required for the completion of the task (up to one order of magnitude with respect to software solutions and up to a speedup factor of 25 with respect to hardware solutions). Finally, run-time reconfiguration capabilities allow to reduce the amount of resources required by the proposed approach.

Communication infrastructure for reconfigurable architectures. Recent advances in VLSI technology show the limits of the classical computation-centric design paradigm. The ever increasing level of integration and complexity in digital electronic systems requires a communication-centric approach for designing high performance systems, where integrable modules (IP-Cores) require high levels of communication. Classical approaches like bus or point-to-point interconnects are no longer sufficient to ensure and support communication requirements. Buses become a bottleneck with the increasing number of integrable modules, while point-to-point interconnects are only feasible for short range applications. A new relevant approach has been defined, namely Network-on-Chip [**D.30**], in which theory and applications of well-known data networks are borrowed in the System-on-Chip context. In this scenario, there is an emerging need of having a methodology that supports the designer in the definition of the best fitting communication infrastructure [**D.24, E.21**]. This scenario can be further extended to support partial dynamic reconfiguration of the Communication Infrastructure (CI), in order to cope either with the changes of the user needs or with the changing environment [**D.28**].

Multi-FPGAs heterogeneous architecture. In this research we consider multi-FPGAs, reconfiguration and system description portability as the processes of specifying and modeling a complete system before it is partitioned and committed to a style/flow of implementation, attempting to obtain a solution which gives the optimal cost, according to a user defined quality of service value, and performance for the application.In the case of a high performance computing cluster employing FPGAs, the reconfigurable elements need to be dynamically re-allocated and reconfigured based on the prevailing workload at a given instance. We particularly target fast configuration and task migration in high performance computing systems, such as server farms. In this research [**E.14**], the main emphasis is on correctness and dependability of joining technologies in the hardware and software domains, on the reconfigurable hardware characteristics, on the heterogeneous architectural description, on the satisfaction of quality of service constraints and, in general, on the exploration of the solution space, in order to evaluate the most effective solutions that are compatible. The main goal of this work is the definition of an environment able to serve several applications sharing the same heterogeneous multi-FPGAs physical architecture. In order to meet this goal several aspects need to be taken under consideration i.e. multi-FPGAs solution Vs reconfigurable one, how to characterized the underlying environment to permit the correct application mapping over it.

2.1.8 Research && Education: how to create a win-win game where research and the students experience are positively influenced one other

Research and Education have been often perceived as a dichotomy. It has often been hard to couple them in a productive and virtuous cycle. I believe that Research can obtain great benefits from Teaching and the other way around [**E.20**]. In particular, involving students in research activities will heavily increase the design and coding power of a research group. On the contrary, from a educative point of view, giving to the student the chance to be involved in real projects will mean giving them the chance to experience real design and development challenges and by guiding them during the design and development we can, in a maieutic way, teach them how to approach real life projects. In such a context it is necessary to provide to the students an environment where they can work and experiment a motivating experience and it is exactly at this point that the DRESD project plays a key-role with its activities [**see http://www.dresd.org/DRESDevents for more information**].

2.2 Program committee, conference organization and revision activities

2.2.1 International Workshops Organization

- **International coordinator**
  International Conference on Industrial and Information System, ICIIS 07 Date: August, 2007

Location: University of Peradeniya, Sri Lanka
Conference Chairman: Janaka Ekanayake
Workshop Chairman: Marco D. Santambrogio
Workshop Title: Reconfigurable Computing

2.2.2 National Workshops, Seminars and Talks Organization

- *Dynamic Reconfiguration in Embedded Systems*, speaker: Markus Koster (Heinz Nixdorf Institute), DEI - Politecnico di Milano, August 2005.
- *Runtime module placement for heterogeneous reconfigurable architecture*, speaker: Markus Koster (Heinz Nixdorf Institute), Politecnico di Milano, August 2005
- *Cinquant'anni di storia informatica. Conta la storia per predire il futuro?*, speaker: Prof. Luigi Dadda, DEI - Politecnico di Milano, October 2006.
- *Spatial Computation and Compiler techniques for configurable Architectures*, speakers: Dr. Alberto Gallini e Dr. Lorenzo Pavesi, DEI - Politecnico di Milano, 2007.
- *IEEE Expert now: Tutorial on-line*, IEEE Delegation, DEI - Politecnico di Milano, September 2007.
- *Alla ricerca della ricerca. Dalla nascita del dipartimento di elettronica ed informazione del Politecnico di Milano ad oggi*, speaker: Prof. Renato Stefanelli, DEI - Politecnico di Milano, November 2007.
- *Innovative Research and Electronic Design Automation: An Industrial Perspective*, speaker: Ing. Alessandro Balboni (EDA Team Manager - Nokia Siemens Networks), DEI - Politecnico di Milano, January 2008.
- *Innovative Design Platforms for Reliable SoCs in Advanced Nanometer Technologies*, speaker: Davide Pandini (Central CAD and Design Solutions - STMicroelectronics), DEI - Politecnico di Milano, March 2008.
- *Partial Dynamic Reconfiguration Workshop*, Nokia Siemens Networks, Cinisello Balsamo, Milano, April 23, 2008.
- *Reconfigurable Computing Italian Workshop*, first Italian Meeting, S01 - Politecnico di Milano, Milano, 19 Dicembre 2008.

2.2.3 International Conferences and Journal Organization

- **Journal Guest editor**
  - Journal of Systems Architecture
    Title: Design Flows and System Architectures for Adaptive Computing on Reconfigurable Platforms.
    Editor: Elsevier
    Guest editors: M. D. Santambrogio, I. Bravo
    References: http://www.elsevier.com/inca/publications/misc/JSASI-AdaptiveComputingTrends.pdf
  - EURASIP Journal on Embedded Systems
    Title: Reconfigurable computing and hardware/software codesign.
    Editor: Hindawi Publishing Corporation
    Guest editors: T. Plaks, M. D. Santambrogio, D. Sciuto
    References: www.hindawi.com/journals/es/si/rcc.pdf
    www.hindawi.com/journals/es/raa.731830.html
- **Members of editorial advisory board:**
  - Title: Dynamic Reconfigurable Network-on-Chip Design: Innovations for Computational Processing and Communication.
    Editor: IGI Global
    Authors: Jih-Sheng Shen, Pao-Ann Hsiung
    References: http://embedded.cs.ccu.edu.tw/ nocbook/

- **Special Session Organization at International Conferences**
  - IEEE International Symposium on Circuits and Systems, ISCAS 07
    Date: May, 2007
    Location: New Orleans, USA
    Conference Chairman: Prof. Magdy Bayoumi, University of Louisiana at Lafayette
    Session Organizer: Marco D. Santambrogio, Donatella Sciuto
    Session Title: Design Methodology For Partial Dynamic Reconfiguration: A New Degree Of Freedom In The HW/SW Codesign Techniques
  - 15th International Conference on Very Large Scale Integration, IFIP VLSI-SoC 2007
    Date: October, 2007
    Location: Atlanta, USA
    Conference Chairman: Vincent John Mooney III
    Session Chairman: Marco D. Santambrogio, Jurgen Becker
    Session Title: Architecture Design Principles
  - IEEE International Symposium on Circuits and Systems, ISCAS 2010
    Date: May 30th - June 2nd, 2010
    Location: New Orleans, USA
    Conference Chairman: Prof. Amara Amara, ISEP, France
    Session Organizer: Marco D. Santambrogio, Luca Benini
    Session Title: New Frontiers in the Design of Communication Infrastructure for Adaptable Systems

2.2.4 Program Co-Chair

- IEEE International Conference on Field Programmable Logic and Applications (FPL): 2010

2.2.5 Program Committee

- IEEE Reconfigurable Architectures Workshop (RAW): 2007, 2008, 2009, and 2010
- IEEE International Conference on Field Programmable Logic and Applications (FPL): 2008, 2009, and 2010
- Southern Conference on Programmable Logic (SPL) Conference: 2008, 2009, 2010, and 2011
- IEEE Field Programmable Technology (FPT): 2007, 2008, 2009, and 2010
- International Symposium on System-on-Chip (SoC): 2009 and 2010
- International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA) Conference: 2006, 2007, 2008, 2009, and 2010
- International Conference on ReConFigurable Computing and FPGAs (ReConFig): 2006, 2008, 2009 and 2010
- SPIE Conference: Microtechnologies for the New Millennium 2009 and 2010
- IEEE Computer Society Annual Symposium on VLSI (ISVLSI): 2009 and 2010
- IEEE/IFIP International Conference on Embedded and Ubiquitous Computing (Embedded Systems and Hardware-Software Codesign Track): 2009 and 2010
- International Workshop on Reconfigurable and Multicore Embedded Systems (WoRMES): 2009
- Workshop on Reconfigurable Computing (WRC): 2010
- IEEE International Conference on Networking, Architecture, and Storage (NAS): 2010
- International Workshop on Highly Efficient Accelerators and Reconfigurable Technologies (HEART): 2010

2.2.6 Session chair at International Conferences

- The 2006 International Conference on Engineering of Reconfigurable Systems and Algorithms, ERSA 06
- IEEE 3rd Southern Conference on Programmable Logic, SPL 07
- IEEE International Parallel and Distributed Processing Symposium, IPDPS'07, IPDPS 2010 - Reconfigurable Architecture Workshop
- IEEE International Symposium on Circuits and Systems, ISCAS 07 and ISCAS 2010
- 3rd International Conference on Information System Security, ICIIS 07

2.2.7 Revision activities

- IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
- IEEE Transaction on Computer-Aided Design (TCAD)
- IEEE Transaction on Computer (TOC)
- IEEE Transactions on Industrial Informatics (TII)
- IEEE Embedded Systems Letters (ESL)
- IEEE Transactions on Signal Processing
- ACM Transaction on Reconfigurable Technology and Systems (TRETS)
- ACM Transactions on Embedded Computing Systems (TECS)
- Journal of Systems Architecture (JSA) - Elsevier
- Integration, the VLSI Journal - Elsevier
- Computers & Electrical Engineering - Elsevier
- International Journal of Circuit Theory and Applications (IJCTA) - Wiley
- Journal of Computer Science and Technology (JCST)
- International Conferences:
  - IEEE International Conference on Field Programmable Logic and Applications (FPL);
  - IEEE Reconfigurable Architectures Workshop (RAW);
  - IEEE Computer Society Annual Symposium on VLSI (ISVLSI);
  - IEEE International Conference on Field-Programmable Technology (FPT);
  - ACM Great Lakes Symposium on VLSI (GLSVLSI);
  - IEEE/IFIP International Conference on Embedded and Ubiquitous Computing;
  - International Workshop on Reconfigurable and Multicore Embedded Systems (WoRMES);
  - IFIP International Conference on Very Large Scale Integration (VLSI-SoC);
  - International Symposium on System-on-Chip (ISSoC);
  - Southern Conference on Programmable Logic (SPL) Conference;
  - Engineering of Reconfigurable Systems and Algorithms (ERSA);
  - International Conference on Green Circuits and Systems (ICGCS).

2.3 Invited talks and paper presentations

- **Invited talks**
  - *Dynamic Reconfigurability in Embedded System Design.*
    Speaker: M. D. Santambrogio
    Heinz Nixdorf Institute, Paderborn, Germany, January 26, 2006.
  - *Partial Dynamic Reconfiguration: Basic Concepts.*
    Speaker: M. D. Santambrogio
    Nokia Siemens Networks, Cinisello Balsamo, Milano, April 23, 2008.
  - *Partial Dynamic Reconfiguration: Real Needs and Limits.*
    Speaker: M. D. Santambrogio
    Nokia Siemens Networks, Cinisello Balsamo, Milano, April 23, 2008.
  - *Design Flow for System-on-Programmable Chip.*
    Speaker: M. D. Santambrogio
    Nokia Siemens Networks, Cinisello Balsamo, Milano, April 23, 2008.
  - *Reconfiguration technologies and DRESD contribution.*
    Speaker: M. D. Santambrogio
    Nokia Siemens Networks, Cinisello Balsamo, Milano, April 23, 2008.
  - *A parallel-serial decimal multiplier architecture.*
    L. Dadda, M. D. Santambrogio
    4th Logic Synthesis Italian Day, Politecnico di Milano, Milano, June 30, 2008.
  - *From Reconfigurable Architectures to Self-Adaptive Autonomic Systems.* - Keynote Speech
    Speaker: M. D. Santambrogio
    International Workshop on Reconfigurable and Multicore Embedded System, August 29, 2009.
  - *Enabling Technologies For Self-Aware Adaptive Systems.*
    M. D. Santambrogio, H. Hoffmann, J. Eastep, J. E. Miller, A. Agarwal.
    NASA/ESA Conference on Adaptive Hardware and Systems, AHS 2010, Anaheim California, USA, June 15 - 18, 2010
- **Paper presentations**
  - 25-28 September 2005, Washington- USA, IEEE International SoC Conference (*Operating system support for dynamically reconfigurable SoC architectures*).
  - 25-26 April 2006, Rodi - Grecia, IEEE RAW - 13th Reconfigurable Architectures Workshop (*VHDL to FPGA automatic IPCore generation: A case study on Xilinx design flow*).
  - 26-29 June 2006, Las Vegas - Nevada, ERSA - Engineering of Reconfigurable Systems and Algorithms (*SyCERS: a SystemC design exploration framework for SoC reconfigurable architecture*; *Synthesis of Object Oriented Models on Reconfigurable Hardware*).
  - 28-30 August, Madrid - Spagna, IEEE FPL - 16th International Conference on Field Programmable Logic and Applications (*Partial dynamic reconfiguration: the Caronte approach. A new degree of freedom in the HW/SW codesign.*).
  - 19-22 September 2006, Darmstadt - Germania, FDL - Forum on Specification and Design Languages (*Adaptive Metrics for System-Level Functional Partitioning.*).
  - 16-18 Ottobre 2006, Nizza - Francia, IFIP VLSI SoC Conference - 14th IFIP International Conference on Very Large Scale Integration (*A graph-coloring approach to the allocation and tasks scheduling for reconfigurable architectures.*; *Fast IP-Core Generation in a Partial Dynamic Reconfiguration Workflow*; *The Caronte Approach for Dynamically Reconfigurable Systems*).
  - 13-15 December 2006, Bangkok - Thailandia, IEEE FPT - International Conference on Field-Programmable Technology (*Combining Hardware Reconfiguration and Adaptive Computation for a Novel SoC Design Methodology*).

– February 2007, Mar del Plata, Agentina, IEEE 3rd Southern Conference on Programmable Logic, SPL 07 (*A genetic algorithm based solution for dynamically reconfigurable modules allocation*; *RoadRunner and IPGen: a combined solution to speedup the reconfigurable architectures design*; *A novel hardware/software codesign methodology based on dynamic reconfiguration with ImpulseC and CoDeveloper*).

– 11-13 March 2007, Stresa-Lago Maggiore, Italia, Great Lake Symposium VLSI, GLSVLSI 07 (*SEU Mitigation for SRAM Based FPGAs through Dynamic Partial Reconfiguration.*).

– 26-27 March 2007, Long Beach - CA - USA, IEEE RAW - 14th Reconfigurable Architectures Workshop (*Partial dynamic reconfiguration in a multi-FPGAs clustered architecture based on Linux.*).

– 27-30 May 2007, New Orleans- USA, IEEE International Symposium on Circuits and Systems, ISCAS 07 (*DRESD. Dynamic Reconfigurability in Embedded System Design.*).

– 25-29 June 2007, Las Vegas - Nevada, ERSA - Engineering of Reconfigurable Systems and Algorithms (*Task Partitioning for the Scheduling on Reconfigurable Systems driven by Specification Self-Similarity.* - [B.32]; *Evolvable Hardware: a Functional Level Evolution Framework based on Impulse C.*; *Exploring Partial Reconfiguration for Mitigating SEU faults in SRAM-Based FPGAs.*).

– 8-11 August 2007, Sri Lanka, International Conference on Industrial and Information System, ICIIS 07 (*Data memory management in partial dynamically reconfigurable systems.*).

– 10-14 March 2008, Monaco - Germania, Design, Automation and Test in Europe - DATE (*Task scheduling with configuration prefetching and anti-fragmentation techniques on dynamically reconfigurable systems.*)

– 7-9 April 2008, Montepellier - Francia, IEEE Computer Society Annual Symposium on VLSI - ISVLSI (*Core allocation and relocation management for a self dynamically reconfigurable architecture.*)

– 14-15 April 2008, Miami - FL - USA, IEEE RAW - 15th Reconfigurable Architectures Workshop (*A Design Flow Tailored for Self Dynamic Reconfigurable Architecture.*; *HARPE: a Harvard-based Processing Element Tailored for Partial Dynamic Reconfigurable Architectures.*).

– May 10 - 12, 2009, Boston, Massachusetts, Great Lake Symposium VLSI (*Task Graph Scheduling for Reconfigurable Architectures driven by Reconfigurations Hiding and Resources Reuse.*)

– May 10 - 12, 2009, Boston, Massachusetts, Great Lake Symposium VLSI (*Reconfigurable NoC Design Flow for Multiple Applications Run-Time Mapping on FPGA Devices.*)

– May 25 - 29, 2009, Rome - Italy, 16th Reconfigurable Architectures Workshop (*On-Line Task Management for a Reconfigurable Cryptographic Architecture.*)

3 Teaching Activity

3.1 Courses

- University: Politecnico di Milano (Milano, Italy):
  - Course: Informatica B - Undergraduate Course
    Teacher: prof. M. D. Santambrogio
    Academic Year: 2010/2011
  - Course: Projects of Ingegneria Informatica - Undergraduate Course
    Teacher: prof. M. D. Santambrogio
    Academic Year: 09/10, 08/09
- University: University of Illinois at Chicago (Chicago, Illinois - USA):
  - Course: Advanced Computer Architecture (CS/ECE/MENG 466) - Graduate Course (taught in English)
    Teacher: prof. M. D. Santambrogio
    Academic Year: 09/10

3.2 Teaching Assistantships

- University: Politecnico di Milano (Milano, Italy):
  - Course: High Performance and Processors and Systems - Graduate course (taught in English)
    Teacher: prof. D. Sciuto
    Academic Year: 09/10, 07/08, 06/07
  - Course: Architettura Avanzata dei Calcolatori (Advanced Computer Architecture) - Graduate Course
    Teacher: prof. D. Sciuto
    Academic Year: 2010/2011
  - Course: Architettura dei Calcolatori (Computer Architecture) - Graduate Course
    Teacher: prof. D. Sciuto
    Academic Year: 08/09, 07/08, 06/07
  - Course: Reti Logiche A - Undergraduate Course
    Teacher: prof. C. Bolchini
    Academic Year: 08/09, 07/08, 06/07, 05/06, 04/05
  - Course: Reti Logiche B - Undergraduate Course
    Teacher: prof. F. Salice
    Academic Year: 05/06
  - Course: Informatica I - Undergraduate Course
    Teacher: prof. C. Bolchini
    Academic Year: 05/06
- University: Advanced Learning and Research Institute, master in Embedded Systems (Lugano, Switzerland):
  - Course: Design Technologies - Graduate course (taught in English)
    Teacher: prof. G. De Micheli
    Academic Year: 07/08, 06/07
  - Course: Validation and Verification - Graduate course (taught in English)
    Teacher: prof. F. Somenzi
    Academic Year: 06/07, 05/06, 04/05
- University: Universtia' degli Studi di Milano (Crema, Italy)
  - Course: Sistemi Operativi (Operating System) - Undergraduate Course
    Teacher: prof. V. Piuri
    Academic Year: 08/09, 07/08, 06/07, 05/06

3.3 Theses Supervision

- **Advisor of the following Master Theses at UIC:**

  - *Design Methodologies for Dynamic Reconfigurable Multi-FPGA Systems* - Student: A. Panella. University of Illinois at Chicago, May 2008;
  - *Operating System Support for Core Management in a Dynamic Reconfigurable Environment* - Student: I. Beretta. University of Illinois at Chicago, May 2008;
  - *Management and Analysis of Bitstreams Generators for Xilinx FPGAs* - Student: D. Candiloro. University of Illinois at Chicago, May 2008;
  - *Time-driven reconfiguration-aware floorplacer* - Student: A. Montone. University of Illinois at Chicago, May 2008;
  - *1D and 2D Bitstream Relocation for Partially Dynamically Reconfigurable Architecture* - Student: M. Novati. University of Illinois at Chicago, May 2008;
  - *DFDK: A Novel Reasoning-Centric Design Methodology for FPGA-Based Systems* - Student: M. Murgida. University of Illinois at Chicago, May 2009;
  - *Application heartbeats: a technique for enhancing system self-adaptability* - Student: M. Triverio. University of Illinois at Chicago, May 2010;
  - *Adaptive Systems Implementation via Software Hot-Swap Mechanisms* - Student: F. Sironi. University of Illinois at Chicago, May 2010;
  - *Self-Adaptive Synchronization Mechanisms for Runtime Application Performance Improvement* - Student: A. Nsamedjeu. University of Illinois at Chicago, May 2010;

- **Advisor of the following Master Theses at Politecnico di Milano:**

  - *Trojan-Free FPGA Circuits using ECC-based Functional Trust-Checking* - Student: M. Maggioni. Politecnico di Milano, July 2010;
  - *A Reactive FPGA-Based Self-Adaptive System* - Student: D. Mattasoglio. Politecnico di Milano, July 2010;

- **Advisor of Bachelor Theses at Politecnico di Milano, from the academic year 2008 - 2009:** 23

- **Co-Advisor of the following Master Theses:**
  From the academic year 2004 - 2005 until today, Marco D. Santambrogio has been the co-advisor of 19 students for their M.Sc. thesis works at Politecnico di Milano

- **Co-Advisor of the following Bachelor Theses:**
  From the academic year 2004 - 2005 until today, Marco D. Santambrogio has been the co-advisor of more than 100 students for their bachelor thesis works at Politecnico di Milano

4 Awards and Research Grants

- **Awards:**
  - Co author of the **Best paper award**: 15th International Conference on Very Large Scale Integration, IFIP VLSI-SoC 2007 (*ReCPU: a Parallel and Pipelined Architecture for Regular Expression Matching* [D.17])
  - **Dimitri N. Chorafas PhD Thesis Award** from the Chorafas Foundation (Berne, Switzerland)for the best PhD Theses in "'Systems Engineering and Information Technology"', May 2008. Thesis title: *Hardware/Software codesign methodologies for dynamically reconfigurable systems* ([E.1])
  - December, 2008. He has been awarded a **Progetto Rocca Postdoc Fellowship at MIT**.
  - Co-author of the Best Paper Award Finalist, IEEE International Conference on Field Programmable Logic and Applications (FPL) 2009
  - Co-author of the **Best Student Paper award sponsored by IEEE TCPP**: 7th IEEE International Conference on Autonomic Computing (ICAC) 2010 (*Smartlocks: Lock Acquisition Scheduling for Self-Aware Synchronization* [D.44])
- **Research Grant:**
  - **HiPEAC Collaboration Grant**. Title of the research: Self-Aware Reconfigurable Computing Systems for Energy Saving and Performance Enhancement, November 2010 - December 2011
  - **HiPEAC Collaboration Grant**. Title of the research: Self-aware and autonomic system, July 2009
  - **Swiss NSF Research Project (Division II)**. Project title: *Dynamically Adaptive Architectures for Nomadic Embedded Systems.* Partners: EPFL, Prof. David Atienza, in cooperation with Politecnico di Milano (IT): Prof. Donatella Sciuto and Dr. Marco D. Santambrogio. Period: 02/2010 - 01/2013.

5 Publications

5.1 International Journals

A.1 T. P. Plaks, M. D. SANTAMBROGIO, D. Sciuto.
Reconfigurable Computing and Hardware/Software Codesign.
EURASIP Journal on Embedded Systems, vol. 2008, Article ID 731830
Editorial.

A.2 S. Corbetta, M. Morandi, M. Novati, M. D. SANTAMBROGIO, D.Sciuto, P. Spoletini.
Internal and External Bitstream Relocation for Partial Dynamic Reconfiguration.
IEEE Transaction on Very Large Scale Integration (VLSI) Systems, vol.17, no.11, pp.1650-1654, Nov. 2009

A.3 R. Cordone, F. Redaelli, M.A. Redaelli, M. D. SANTAMBROGIO, D.Sciuto.
Partitioning and Scheduling of Task Graphs on Partially Dynamically Reconfigurable FPGAs.
IEEE Transactions on Computer-Aided Design (TCAD) of Integrated Circuits and Systems, vol. 28, no. 5, pp. 662 - 675, May 2009

A.4 A. Montone, M. D. SANTAMBROGIO, D. Sciuto S. Ogrenci Memik.
Placement and Floorplanning in Dynamically Reconfigurable FPGAs.
ACM Transactions on Reconfigurable Technology and Systems, *accepted - to appear.*

A.5 M. D. SANTAMBROGIO, R. Stefanelli.
A New Compact SD2 Positive Integer Triangular Array Division Circuit.
IEEE Transaction on Very Large Scale Integration (VLSI) Systems, *accepted to appear - available online.*

A.6 F. Redaelli, M. D. SANTAMBROGIO, S. Ogrenci Memik.
An ILP formulation for the Task Graph Scheduling Problem tailored to bi-dimensional Reconfigurable Architectures.
International Journal of Reconfigurable Computing, vol. 2009, Article ID 541067, 12 pages, 2009. doi:10.1155/2009/541067.

A.7 M. D. SANTAMBROGIO.
From reconfigurable architectures to self-adaptive autonomic systems
Journal of Embedded Systems, Special Issue on Reconfigurable and Multicore Embedded Systems, 2010, *accepted - to appear.*

5.2 Books

B.1 Pao-Ann Hsiung, M. D. SANTAMBROGIO, Chun-Hsian Huang.
Reconfigurable System Design and Verification
Taylor & Francis/CRC Press, January 2009.

5.3 Books chapter

C.1 A. Donato, F. Ferrandi, M. Redaelli, M. D. SANTAMBROGIO, D. Sciuto.
Exploiting partial dynamic reconfiguration for SoC design of complex application on FPGA platforms.
Ricardo Augusto da Luz Reis, Adam Osseiran, Hans-Jorg Pfleiderer (Eds.), VLSI-SoC: From Systems To Silicon, Springer 2007, p.: 87 - 109

C.2 M. Paolieri, I. Bonesana, M. D. SANTAMBROGIO.
ReCPU: a Parallel and Pipelined Architecture for Regular Expression Matching.
R. Reis, V. Mooney and P. Hasler (Eds.), VLSI-SoC: Advanced Topics on Systems on a Chip, Springer 2009, p.: 89 - 108

C.3 V. Rana, C. Sandionigi, M. D. SANTAMBROGIO, D. Sciuto.
An adaptive genetic algorithm for dynamically reconfigurable modules allocation.
R. Reis, V. Mooney and P. Hasler (Eds.), VLSI-SoC: Advanced Topics on Systems on a Chip, Springer 2009, p. 209 - 226

C.4 F. Bruschi, A. Meroni, V. Rana, M. D. SANTAMBROGIO.
A Requirements-Driven Simulation Framework For Communication Infrastructures Design.
Languages for Embedded Systems and their Applications Selected Contributions on Specification, Design, and Verification from FDL08, Springer 2009), p.: 291 - 307

C.5 V. Rana, D. A. Atienza, M. D. SANTAMBROGIO, D. Sciuto, G. De Micheli.
A Reconfigurable Network-on-Chip Architecture for Optimal Multi-Processor SoC Communication, VLSI-SoC: Design Methodologies for SoC and SiP, Springer, p.: 232-250

C.6 V. Rana, M. D. SANTAMBROGIO, S. Corbetta.
Dynamic Reconfigurable NoCs: Characteristics and Performance Issues.
Jih-Sheng Shen Pao-Ann Hsiung (Eds.), Dynamic Reconfigurable Network-on-Chip Design: Innovations for Computational Processing and Communication", IGI Publisher, p.: 158-185

C.7 V. Rana, M. D. SANTAMBROGIO, A. Meroni.
Design Methodologies and Mapping Algorithms for Reconfigurable NoC-based Systems.
Jih-Sheng Shen Pao-Ann Hsiung (Eds.), Dynamic Reconfigurable Network-on-Chip Design: Innovations for Computational Processing and Communication", IGI Publisher, p.: 110-134

5.4 International Conferences

D.1 A. Donato, F. Ferrandi, M. D. SANTAMBROGIO, D. Sciuto.
Operating system support for dynamically reconfigurable SoC architectures.
IEEE International SOC Conference - IEEE-SOCC 2005, proc. p. 235 - 238, Washington, USA, September 25 - 28, 2005

D.2 A. Donato, F. Ferrandi, M. Redaelli, M. D. SANTAMBROGIO, D. Sciuto.
Exploiting partial dynamic reconfiguration for SoC design of complex application on FPGA platforms.
13th IFIP International Conference on Very Large Scale Integration - IFIP VLSI-SOC 2005, proc. p. 179 - 184, Perth, Australia, October 17 - 19, 2005
Selected among the conference best papers and invited for a publication in the book: VLSI-SoC: From Systems To Silicon, Springer ([C.1])

D.3 F. Ferrandi, M. Redaelli, M. D. SANTAMBROGIO, D. Sciuto.
Solving the Coloring Problem to Schedule on Partially Dynamically Reconfigurable Hardware.
13th IFIP International Conference on Very Large Scale Integration - IFIP VLSI-SOC 2005, proc. p. 97 - 102, Perth, Australia, October 17 - 19, 2005

D.4 R. Cordone, F. Ferrandi, G. Palermo, M. D. SANTAMBROGIO, D. Sciuto.
Using Speculative Computation and Parallelizing Techniques to Improve Scheduling of Control based Designs.
11th Asia and South Pacific Design Automation Conference, ASP-DAC 2006, proc. p. 898 - 904, Yokohama, Japan, January 24 - 27, 2006

D.5 S. Borgio, D. Bosisio, M. Monchiero, A. Tumeo, F. Ferrandi, M. D. SANTAMBROGIO, D. Sciuto.
Hardware DWT accelerator for MultiProcessor System On-Chip on FPGA.
In Proceedings of IEEE IC-SAMOS'06 - Embedded Computer Systems: Architectures, MOdeling, and Simulation, proc. p. 107 - 114, Samos, Greece, July 17 - 20, 2006

D.6 C. Amicucci, F. Ferrandi, M. D. SANTAMBROGIO, D. Sciuto.
SyCERS: a SystemC design exploration framework for SoC reconfigurable architecture.
The 2006 International Conference on Engineering of Reconfigurable Systems and Algorithm, ERSA 06, proc. p. 63 - 69, Las Vegas, Nevada, USA, June 26 - 29, 2006

D.7 M. Giorgetta, M. D. SANTAMBROGIO, D. Sciuto, P. Spoletini.
A graph-coloring approach to the allocation and tasks scheduling for reconfigurable architectures.
14th IFIP International Conference on Very Large Scale Integration - IFIP VLSI-SOC 2006, proc. p. 24 - 29, Nice, France, October 16 - 18, 2006

D.8 M. Murgida, A. Panella, V. Rana, M. D. SANTAMBROGIO, D. Sciuto.
Fast IP-Core Generation in a Partial Dynamic Reconfiguration Workflow.
14th IFIP International Conference on Very Large Scale Integration - IFIP VLSI-SOC 2006, proc. p. 74 - 79, Nice, France, October 16 - 18, 2006

D.9 M. D. SANTAMBROGIO.
The Caronte Approach for Dynamically Reconfigurable Systems.
14th IFIP International Conference on Very Large Scale Integration - IFIP VLSI-SOC 2006, proc. p. 1 - 6, Nice, France, October 16 - 18, 2006

D.10 F. Ferrandi, M. Morandi, M. Novati, M. D. SANTAMBROGIO, D. Sciuto.
Dynamic Reconfiguration: Core Relocation via Partial Bitstreams Filtering with Minimal Overhead.
International Symposium on System-on-Chip - SoC 06, proc. p. 33 - 36, Tampere, Finland, November 13 - 16, 2006

D.11 V. Rana, S. Ogrenci Memik, M. D. SANTAMBROGIO, D. Sciuto.
Combining Hardware Reconfiguration and Adaptive Computation for a Novel SoC Design Methodology.
International Conference on Field Programmable Technology - FPT 06, proc. p. 293 - 296, Bangkok, Thailand, December 13 - 15, 2006

D.12 V. Rana, C. Sandionigi, M. D. SANTAMBROGIO.
A genetic algorithm based solution for dynamically reconfigurable modules allocation.
IEEE 3rd Southern Conference on Programmable Logic, SPL 07, proc. p. 183 - 186, Mar del Plata, Argentina, February 26 - 28, 2007

D.13 A. Antola, M. Fracassi, P. Gotti, C. Sandionigi, MARCO D. SANTAMBROGIO.
A novel hardware/software codesign methodology based on dynamic reconfiguration with ImpulseC and CoDeveloper.
IEEE 3rd Southern Conference on Programmable Logic, SPL 07, proc. p. 221 - 224, Mar del Plata, Argentina, February 26 - 28, 2007

D.14 V. Rana, M. D. SANTAMBROGIO, D. Sciuto.
Dynamic Reconfigurability in Embedded System Design.
IEEE International Symposium on Circuits and Systems, ISCAS 07, proc. p. 2734 - 2737, New Orleans, Louisiana, USA, May 27 - 30, 2007

D.15 C. Bolchini, D. Quarta, M. D. SANTAMBROGIO.
SEU Mitigation for SRAM Based FPGAs through Dynamic Partial Reconfiguration.
Great Lake Symposium VLSI, GLSVLSI 07, proc. p. 55-60, Stresa-Lago Maggiore, Italy, March 11 - 13, 2007

D.16 M. D. SANTAMBROGIO, V. Rana , S. Ogrenci Memik, D. Sciuto, U. Acar.
A Novel SoC Design Methodology Combining Adaptive Software and Reconfigurable Hardware.
25th International Conference on Computer-Aided Design, ICCAD 2007, proc. p. 303 - 308, San Josè, California, USA, November 5 - 8, 2007

D.17 M. Paolieri, I. Bonesana, M. D. SANTAMBROGIO.
ReCPU: a Parallel and Pipelined Architecture for Regular Expression Matching.
15th International Conference on Very Large Scale Integration, IFIP VLSI-SoC 2007, proc. p. 19 - 24, Atlanta, Georgia, USA, October 15 - 17, 2007
Best Paper Award IFIP VLSI-SoC 2007
Best papers award and invited for a publication in the book: VLSI-SoC: From Systems To Silicon, Springer ([C.2])

D.18 V. Rana, C. Sandionigi, M. D. SANTAMBROGIO, D. Sciuto.
An adaptive genetic algorithm for dynamically reconfigurable modules allocation.
15th International Conference on Very Large Scale Integration, IFIP VLSI-SoC 2007, proc. p. 128 - 133, Atlanta, Georgia, USA, October 15 - 17, 2007
Selected among the conference best papers and invited for a publication in the book: VLSI-SoC: From Systems To Silicon, Springer ([C.3])

D.19 C. Bolchini, A. Miele, M. D. SANTAMBROGIO.
TMR and Partial Dynamic Reconfiguration to mitigate SEU faults in FPGAs.
22nd IEEE International Symposium on Defect and Fault-Tolerance in VLSI Systems, DFT 07, proc. p. 87 - 95, Rome, Italy, September 26 - 28, 2007

D.20 A. Montone, V. Rana, M. D. SANTAMBROGIO.
Data memory management in partial dynamically reconfigurable systems.
3rd International Conference on Information System Security, ICIIS 07, proc. p. 130, Peradeniya, Sri Lanka, August 8 - 11, 2007

D.21 M. Giani, M. Redaelli, M. D. SANTAMBROGIO, D. Sciuto.
Task Partitioning for the Scheduling on Reconfigurable Systems driven by Specification Self-Similarity.
The 2007 International Conference on Engineering of Reconfigurable Systems and Algorithm, ERSA 07, proc. p. 78 - 84, Las Vegas, Nevada, USA, June 25 - 28, 2007

D.22 C. A. Curino, L. Fossati, V. Rana, F. Redaelli, M. D. SANTAMBROGIO, D. Sciuto.
The Shining embedded system design methodology based on self dynamic reconfigurable architectures.
13th Asia and South Pacific Design Automation Conference, ASP-DAC 08, proc. p. 595 - 600, Seoul, Korea, January 21 - 24, 2008

D.23 A. Cuoccio, P. R. Grassi, V. Rana, M. D. SANTAMBROGIO, D. Sciuto.
A Generation Flow for Self-Reconfiguration Controllers Customization.
4th IEEE International Symposium on Electronic Design, Test and Applications, DELTA 08, proc. p. 279 - 284, Hong Kong, January 23 - 25, 2008

D.24 A. Meroni, V. Rana, M. D. SANTAMBROGIO, D. Sciuto.
A Requirements-Driven Reconfigurable SoC Communication Infrastructure Design Flow.
4th IEEE International Symposium on Electronic Design, Test and Applications, DELTA 08, proc. p. 405 - 409, Hong Kong, January 23 - 25, 2008

D.25 F. Redaelli, M. D. SANTAMBROGIO, D. Sciuto.
Task scheduling with configuration prefetching and anti-fragmentation techniques on dynamically reconfigurable systems.
Design, Automation and Test in Europe, DATE 08, proc. p. 519 - 522, Munich, Germany, March 10 - 14, 2008

D.26 M. Paolieri, I. Bonesana, M. D. SANTAMBROGIO.
An adaptable FPGA-based System for Regular Expression Matching.
Design, Automation and Test in Europe, DATE 08, proc. p. 1262 - 1267, Munich, Germany, March 10 - 14, 2008

D.27 M. Morandi, M. Novati, M. D. SANTAMBROGIO, D. Sciuto.
Core allocation and relocation management for a self dynamically reconfigurable architecture.
IEEE Computer Society Annual Symposium on VLSI, ISVLSI 08, proc. p. 286 - 291, Montpellier, France, April 7 - 9, 2008

D.28 S. Corbetta, V. Rana, M. D. SANTAMBROGIO, D. Sciuto.
A Light-Weight Network-on-Chip Architecture for Dynamically Reconfigurable Systems.
In Proceedings of IEEE IC-SAMOS'08 - Embedded Computer Systems: Architectures, MOdeling, and Simulation, proc. p. 49 - 56, Samos, Greece, July 21 - 24, 2008

D.29 M. D. SANTAMBROGIO, V. Rana, D. Sciuto.
Operating System Support for Online Partial Dynamic Reconfiguration Management.
18th International Conference on Field Programmable Logic and Applications, FPL 08, proc. p. 455 - 458, Heidelberg, Germany, September 8 - 10, 2008

D.30 V. Rana, D. A. Atienza, M. D. SANTAMBROGIO, D. Sciuto, G. De Micheli.
A Reconfigurable Network-on-Chip Architecture for Optimal Multi-Processor SoC Communication.
International Conference on Very Large Scale Integration, IFIP VLSI-SoC 2008, proc. p. 321 - 326, Rhodes Island, Greece, October 13 - 15, 2008
Selected among the conference best papers and invited for a publication in the book: VLSI-SoC, Springer ([C.5])

D.31 F. Redaelli, M. D. SANTAMBROGIO, S. Ogrenci Memik.
An ILP formulation for the Task Graph Scheduling Problem tailored to bi-dimensional Reconfigurable Architectures
ReConFig 2008, proc. p. 97 - 102, Cancun, Mexico, December 3 - 5, 2008
Selected among the conference best papers and invited for a publication in the International Journal of Reconfigurable Computing ([A.4])

D.32 A. Montone, F. Redaelli, M. D. SANTAMBROGIO, S. Ogrenci Memik.
A Reconfiguration-aware Floorplacer for FPGAs
ReConFig 2008, proc. p. 109 - 114, Cancun, Mexico, December 3 - 5, 2008

D.33 F. Cancarè, M. D. SANTAMBROGIO, D. Sciuto.
An Application-centered Design Flow for Self Reconfigurable Systems Implementation.
14th Asia and South Pacific Design Automation Conference, ASP-DAC 2009, proc. p. 248 - 253, Yokohama, Japan, January 19 - 22, 2009

D.34 M. D. SANTAMBROGIO, Massimo Redaelli, Marco Maggioni.
Task Graph Scheduling for Reconfigurable Architectures driven by Reconfigurations Hiding and Resources Reuse.
Great Lake Symposium VLSI, GLSVLSI 09, proc. p. 21 - 26, Boston, Massachusetts, May 10 - 12, 2009

D.35 P. R. Grassi, M. D. SANTAMBROGIO, J. Hagemeyer, C. Pohl, M. Porrmann.
SiLLis: A Simplified Language for Monitoring and Debugging of Reconfigurable Systems.
The 2009 International Conference on Engineering of Reconfigurable Systems and Algorithm, ERSA 09, proc. p. 174 - 180, Las Vegas, Nevada, USA, July 13 - 16, 2009

D.36 M. D. SANTAMBROGIO, M. Morandi, M. Novati, D. Sciuto.
A Runtime Relocation Based Workflow for Self Dynamic Reconfigurable Systems Design.
19th International Conference on Field Programmable Logic and Applications, FPL 09, proc. p. 86 - 91, Prague, Czech Republic, August 31 - September 2, 2009

D.37 V. Rana, S. Murali, D. Atienza, M. D. SANTAMBROGIO, L. Benini, D. Sciuto.
Minimization of the reconfiguration latency for the mapping of applications on FPGA-based systems.
The International Conference on Hardware-Software Codesign and System Synthesis, CODES+ISSS 09, proc. p. 325 - 334, Grenoble, France, October 11 - 16, 2009

D.38 F. Redaelli, M. D. SANTAMBROGIO, V. Rana, S. Ogrenci Memik.
Scheduling and 2D Placement Heuristics for Partially Reconfigurable Systems.
International Conference on Field Programmable Technology - FPT 09, proc. p. 223 - 230, Sydney, Australia, December 9 - 11, 2009

D.39 I. Beretta, V. Rana, D. Atienza, M. D. SANTAMBROGIO, D. Sciuto .
Run-time Applications Mapping on Fine-Grained Reconfigurable Embedded Systems.
International Conference on Microelectronics - ICM 09, proc. p. 151-154, Marrakech, Morocco, December 19 - 22, 2009
Invited Talk

D.40 V. Rana, M. D. SANTAMBROGIO, S. Corbetta, D. Sciuto.
Multiple Communication–Domains Design in FPGA–Based Systems–on–Chip.
International conference on Design & Technology of Integrated Systems in nanoscale era - DTISÕ10, proc. 1 - 6, Hammamet, Tunisia, March 23 - 25, 2010

D.41 F. Cancaré, M. D. SANTAMBROGIO, D. Sciuto.
A Direct Bitstream Manipulation Approach for Virtex4-based Evolvable Systems.
IEEE International Symposium on Circuits and Systems - ISCAS 2010, proc. p. 853 - 856 , Paris, France, May 30 - June 2, 2010

D.42 Paolo R. Grassi, Christoph Puttmann, M. D. SANTAMBROGIO, Mario Porrmann, Ulrich Rückert.
High Level Specification of Embedded Listeners for Monitoring of Network-on-Chips.
IEEE International Symposium on Circuits and Systems - ISCAS 2010, proc. p. 3333 - 3336, Paris, France, May 30 - June 2, 2010

D.43 M. D. SANTAMBROGIO, H. Hoffmann, J. Eastep, J. E. Miller, A. Agarwal.
Enabling Technologies For Self-Aware Adaptive Systems.
NASA/ESA Conference on Adaptive Hardware and Systems, AHS 2010, proc. p. 149 - 156, Anaheim California, USA, June 15 - 18, 2010

D.44 J. Eastep, D. Wingate, M. D. SANTAMBROGIO, A. Agarwal.
Smartlocks: Lock Acquisition Scheduling for Self-Aware Synchronization.
7th IEEE International Conference on Autonomic Computing, ICAC 2010, proc. p. 215 - 224, Washington, DC, USA, June 7 - 11, 2010
Recipient of the Best Student Paper award sponsored by IEEE TCPP

D.45 H. Hoffmann, J. Eastep, M. D. SANTAMBROGIO, J. Miller, A. Agarwal.
Application Heartbeats. A Generic Interface for Specifying Program Performance and Goals in Autonomous Computing Environments.
7th IEEE International Conference on Autonomic Computing, ICAC 2010, proc. p. 79 - 88, Washington, DC, USA, June 7 - 11, 2010

D.46 F. Sironi, M. Triverio, H. Hoffmann, M. Maggio, M. D. SANTAMBROGIO.
Self-Aware Adaptation in FPGA-based Systems.
20th IEEE International Conference on Field Programmable Logic and Applications, FPL 2010, proc. p. 187-192, Milan, Italy, August 31 - September 2, 2010

D.47 M. Maggio, H. Hoffmann, M. D. SANTAMBROGIO, A. Agarwal, A. Leva.
Controlling software applications via resource allocation within the Heartbeats framework
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