

CURRICULUM VITÆ

MARCO D. SANTAMBROGIO

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1 PERSONAL DATA

1.1 General data

Name Marco Domenico

Surname Santambrogio

Date of birth November 4, 1977

Place of birth Monza (MB) - Italy

Citizenship Italian

Marital status Married

Office @ PoliMi Dipartimento di Elettronica e Informazione
Politecnico di Milano
Via G. Ponzio 34/5
Milano, Italy 20133

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1.2 Publications

- SCOPUS Author ID: 11540913800 - <https://www.scopus.com/authid/detail.uri?authorId=11540913800>
h-index: 28 @ Apr 2025
- Google Scholar: <https://scholar.google.com/citations?user=Dr2SsKIAAAAJ>
h-index: 43, i10-index: 51 @ Apr 2025
- ORCID: 0000-0002-9883-9693 - <https://orcid.org/0000-0002-9883-9693>
- DBLP: http://dblp.uni-trier.de/pers/hd/s/Santambrogio:Marco_D=.html
- Research Gate: https://www.researchgate.net/profile/Marco_Santambrogio

1.3 Academic positions

- 9/2023 - ...** Full Professor at the Dipartimento di Elettronica ed Informazione of Politecnico di Milano (Milano, Italy).
- 2/2018 - ...** Associate Professor at the Dipartimento di Elettronica ed Informazione of Politecnico di Milano (Milano, Italy).
- 12/2009 - ...** Adjunct Professor in the College of Engineering of University of Illinois at Chicago (Chicago, Illinois, USA).
- 2/2011 - 1/2018** Assistant Professor (with tenure) at the Dipartimento di Elettronica ed Informazione of Politecnico di Milano (Milano, Italy).
- 03/2010 - 02/2014** Research Affiliate at Massachusetts Institute of Technology - Computer Science and Artificial Intelligence Laboratory (Cambridge, MA - USA).
- 11/2009 - 1/2011** Postdoc/Research Assistant at the Dipartimento di Elettronica ed Informazione of Politecnico di Milano (Milano, Italy).
- 02/2009 - 02/2010** Postdoc Fellow (research : Self-Aware Computing Systems.) at Massachusetts Institute of Technology - Computer Science and Artificial Intelligence Laboratory (Cambridge, MA - USA).

- 07/2008 - 10/2009** Research Assistant (research program: Metodologie di progetto di sistemi informatici hardware e software. (Design methodologies for hardware and software IT systems.)) at the Dipartimento di Elettronica ed Informazione of Politecnico di Milano (Milano, Italy).
- 03/2008-07/2008** Research Assistant (research program: Analisi e definizione di possibili scenari applicativi di nuovi sistemi riconfigurabili. (Analysis and definition of applicative scenarios for novel reconfigurable technologies.)) at the Dipartimento di Elettronica ed Informazione of Politecnico di Milano (Milano, Italy).
- 03/2005-02/2008** PhD Student in the Computer Engineering and Automation program at the Dipartimento di Elettronica ed Informazione of Politecnico di Milano (Milano, Italy).
- 11/2004-03/2005** Research Assistant (research program: Definizione di un flusso di design per sistemi riconfigurabili basati su FPGA della Xilinx. (Definition of a novel design flow for Xilinx FPGA-based reconfigurable systems.)) at the Dipartimento di Elettronica ed Informazione of Politecnico di Milano (Milano, Italy).

1.4 Affiliations

- Since 2013** Senior Member of the Association for Computing Machinery (ACM)
- Since 2011** Senior Member of the Institute of Electrical and Electronic Engineers (IEEE)
- Since 2009** Member of the Italian Scientists and Scholars of North America Foundation (ISSNAF)
- Since 2008** Member of HiPEAC Reconfigurable Computing Cluster
- Since 2008** Member of HipEAC, European Network of Excellence on High Performance and Embedded Architecture and Compilation
- Since 2008** Member of the Association for Computing Machinery (ACM)
- Since 2008** Member of the IEEE Circuits and Systems Society (CAS)
- Since 2008** Member of the IEEE Computer Society (CS)
- Since 2005** Member of the Institute of Electrical and Electronic Engineers (IEEE)

1.5 Education

- 15 May, 2008** **PhD in Information Engineering**
 DIPARTIMENTO DI ELETTRONICA ED INFORMAZIONE, POLITECNICO DI MILANO
 PhD Thesis: *Hardware/Software codesign methodologies for dynamically reconfigurable systems.*
 Advisor: Prof. D. Sciuto. Tutor: Prof. F. Ferrandi
- June 2004** **Master of Science in Computer Science**
 UNIVERSITY OF ILLINOIS AT CHICAGO, CHICAGO, ILLINOIS, USA
 Master Thesis: *Dynamic Reconfigurability in Embedded System Design. A Model for the Dynamic Reconfiguration.*
 Advisor: Prof. John Lillis.
- April 2004** **Laurea (MSc equivalent) in Computer Engineering**
 POLITECNICO DI MILANO
 Thesis: *A Methodology for Dynamic Reconfigurability in Embedded System Design.*
 Advisor: Prof. D. Sciuto.

1.6 Visiting periods

- Postdoc Fellow, Massachusetts Institute of Technology, February 2009 - February 2010
- Visiting researcher, Heinz Nixdorf Institute, January 2009
- Invited researcher, Northwestern University, April - May 2007

- Invited researcher, Northwestern University, February - June 2006
- Visiting researcher, Heinz Nixdorf Institute, January 2006
- MSc Student, University of Illinois at Chicago, 2002

1.7 Service Activities

- Service Activities @ IEEE

Nov 2019 - ... Chair - elected - of the IEEE Italian Chapter of the Computer Society

2015 - 2019 Vice-Chair - elected - of the IEEE Italian Chapter of the Computer Society

Since 2016 Member of the IEEE CS Member & Geographic Activities Board

Since 2016 Chair of the IEEE CS ARC Larson Paper Prize

Since 2013 Member of the IEEE Italy Section as Student Activities Coordinator.

2012 - 2015 Member of the IEEE CS Student Awards Committee (SAC).

Since 2012 Member of the IEEE CS Awards and Recognition Committee (ARC) - <https://www.computer.org/web/chapters/mga-board>

- Service Activities @ Politecnico di Milano

Sept 2019 - ... Politecnico di Milano Director for the PoliMi-UIC Double Degree Program

May 2019 - ... Coordinator for the Computer Eng. track for the PoliMi-UIC Double Degree Program

2017 - ... Member of the organizing committee of the *Innovation in Teaching Activities Initiative* for DEIB

2013 - 2015 Member of the organizing committee of the OpenHouse event (Information Technology Section)

2010 - ... MicroLAB Director (until 2012), NECSTLab Founder and Director

2011 - ... Founder and head of the Rocca Fellows community

2010 - ... Organizer of the OpenDay event on behalf of the DEIB Information Technology Section

2008 - 2012 Founder and head of the PhDEI *Association*.

07/2005 - 12/2006 Head of the ICT area and member of the managing board of ISF-MI Association.

July 2005 Co-founder of Engineer Without Border Milano (Ingegneria Senza Frontiere ISF-MI).

- Other Service Activities

2009 - 2012 Member of the MIT Postdoctoral Advisory Council.

2009 - 2012 Member of the National Postdoctoral Association (NAP).

01/2001- 04/2001 Head of the IT area, for Caritas Ambrosiana and CeLIM, of two humanitarian missions in Kosovo (Jacova e Pristina)

02/2000 - 12/2000 Civil service at CeLIM NGO.

1.8 References

In the following, a list of persons (in alphabetical order) who could provide a reference letter:

- Anant Agarwal, CEO EDX, FULL PROFESSOR, Massachusetts Institute of Technology, agarwal@csail.mit.edu
- Jurgen Becker, Full Professor, Karlsruhe Institute of Technology, jurgen.becker@kit.edu
- John Kubiawicz, Full Professor, UC BERKELEY, kubitron@cs.berkeley.edu
- Viktor Prasanna, Full Professor, University of Southern California, prasanna@usc.edu

1.9 Summary of the main achievements

- **2012 - ...** NECSTLab Founder and Director. The NECSTLab described in number
 - **25 PhD students**, first one graduated in 2014;
 - Private funding from companies for a total of **934K EUR** in income, starting in 2016;
 - Definition and teaching of **~ 20 soft skills and technical (e.g. FPGA design, GPU programming) courses**, for a total of **~ 70 editions** in the Innovative Teaching Activity of the Politecnico di Milano and open to all the Politecnico students, since 2018;
 - Involvement of **~100** new students each year in the lab activities;
- **Nov 2019 - ...** Chair elected of the **IEEE Italian Chapter of the Computer Society**
- **2015 - 2019** Vice-Chair elected of the **IEEE Italian Chapter of the Computer Society**
- Founder of **3 startups**, and a **fourth** one under constitution
- Creator of **7 patents**
- **3 editorial advisory board memberships** of **3 Q1 ranked** journals;
- Scientific Productivity: 300+ publications (339 entries on Scopus, 503 co-authors according to Scopus):
- Author/Co-author of **15 top-ranked Q1 journal papers**: [1, 2, 3, 4, 5, 6, 8, 19, 26, 29, 30, 34, 37, 40, 41] (including IEEE Transactions on Parallel and Distributed Systems, IEEE Transactions on Emerging Topics in Computing, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, IEEE Micro, ACM Transactions on Autonomous and Adaptive Systems, IEEE Transactions on Control Systems Technology, and ACM Computing Surveys (CSUR) from SCIMAGO ([HTTP://SCIMAGOJR.COM](http://scimagojr.com)))
- Author/Co-author of 250+ scientific publications on peer-reviewed conferences including 57 top-level A1/A2 Class 1 conferences (ASP-DAC, CODESS+ISSS, DAC, DATE, FCCM, FPGA, FPL, ICAC, ICCAD, IPDPS, ISCAS, OSDI, PACT, PPOPP, UbiComp) from Conference Ranks ([HTTP://WWW.CONFERENCERRANKS.COM/#DATA](http://www.conferencerranks.com/#DATA)).
- Publication Impact:
 - Based on Google Scholar: h-index 41, citations 6025
 - Based on Scopus: h-index 28, citations 3322
 - Based on SciVal: h-index 28

2 SCIENTIFIC ACTIVITIES

2.1 International Conferences and Journal Organization

To summarise the main achievements in this section, I would like to highlight the following:

- **3 editorial advisory board memberships** of **3 Q1 ranked** journals;
- General chair of **5** conferences;
- Steering Committee member of **5** conferences;
- Program chair, vice-chairs of **10** conferences;
- **9** invited talks, among which **3 at A1 conferences** and **1 at A2 conference**.

2.1.1 Journal Editorial Activities

- **Editorial advisory board members:**

- Title: IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)
Ranked Q1 from SCIMAGO (www.scimagojr.com, (<https://www.scimagojr.com/journalsearch.php?q=27724&tip=sid&clean=0>) Editor: IEEE
References: <https://ieeeced.org/publication/tcad-publication/committee/tcad-editorial-board>
From: Sept, 2022
- Title: IEEE Transactions on Parallel and Distributed Systems (IEEE TPDS)
Ranked Q1 from SCIMAGO (www.scimagojr.com, (<https://www.scimagojr.com/journalsearch.php?q=26098&tip=sid&clean=0>) Editor: IEEE
References: <https://www.computer.org/csdl/journal/td>
From: Sept, 2018
- Title: Elsevier Editorial Board of Big Data Research, Editor of the area Cyber-Physical Systems
Ranked Q1 from SCIMAGO (www.scimagojr.com, (<https://www.scimagojr.com/journalsearch.php?q=21100356018&tip=sid&clean=0>) Editor: Elsevier
References: <http://www.journals.elsevier.com/big-data-research/editorial-board/>
From: Dec 17, 2013

- **Journal Special Issue Editor**

- ACM Transactions on Reconfigurable Technology and Systems - Special section on the 22nd Reconfigurable Architectures Workshop (RAW 2014)
- ACM Transactions on Reconfigurable Technology and Systems - Special section on the 10th International Symposium on Reconfigurable Computing: Architectures, Tools, and Applications (ARC 2014)
- Elsevier Journal on Future Generation Computer Systems (FGCS) - Special issue on the 10th International Conference on Embedded and Ubiquitous Computing (EUC 2012) (special session title: Multicore and Many-core Architectures for Future Generation Embedded)

- **Journal Guest Editor**

- Microprocessor and Microsystems Journal, Special Issue
Title: Embedded Multicore Systems: Architecture, Performance and Application.
Editor: Elsevier
Guest editors: M. Chang, P.A. Hsiung, M. D. Santambrogio, W. H. Lee
References: http://www.elsevierscitech.com/cfp/Call_for_papers_Multicore_Embedded.pdf
- EURASIP Journal of Reconfigurable Computing
Title: Self-Awareness in Reconfigurable Computing Systems.
Editor: Hindawi Publishing Corporation
Guest editors: T. Becker, M. D. Santambrogio, M. Happe, M. Platzner,
References: <http://www.hindawi.com/journals/ijrc/si/807910/cfp/>

- International Journal on Reconfigurable Computing, Special Issue
Title: Selected Papers from the International Conference on Reconfigurable Computing and FPGAs (ReConFig'10)
Editor: Hindawi Publishing Corporation
- Journal of Systems Architecture
Title: Design Flows and System Architectures for Adaptive Computing on Reconfigurable Platforms.
Editor: Elsevier
Guest editors: M. D. Santambrogio, I. Bravo
References: <http://www.elsevier.com/inca/publications/misc/JSASI-AdaptiveComputingTrends.pdf>
- EURASIP Journal on Embedded Systems
Title: Reconfigurable computing and hardware/software codesign.
Editor: Hindawi Publishing Corporation
Guest editors: T. Plaks, M. D. Santambrogio, D. Sciuto
References: www.hindawi.com/journals/es/si/rcc.pdf
www.hindawi.com/journals/es/raa.731830.html

2.2 Program committee, conference organization and revision activities

2.2.1 Steering Committee

- IEEE International Parallel and Distributed Processing Symposium (IPDPS): since 2024
- IEEE Reconfigurable Architectures Workshop (RAW): since 2023
- IEEE International Conference on Cyber, Physical and Social Computing (CPSCoM): 2017
- Embedded Operating System Workshop (EWiLi): 2016, 2017
- IEEE International Conference on Networking, Architecture, and Storage (NAS): 2014, 2015

2.2.2 General Chair

- IEEE International Parallel and Distributed Processing Symposium (IPDPS), Ranked A: : 2025
- Annual IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP), Ranked B1: 2018
- IEEE/IFIP International Conference on Embedded and Ubiquitous Computing (EUC), Ranked B1: 2014
- IEEE International Symposium on Parallel and Distributed Processing with Applications (ISPA), Ranked B3: 2014
- IEEE International Conference on Cyber, Physical and Social Computing (CPSCoM): 2013

2.2.3 Program Chair

- IEEE International Conference on Field Programmable Logic and Applications (FPL), Ranked A2: 2010 (226 submitted papers, 60 regular papers), 2017
- IEEE International Conference on Smart City (SmartCity): 2016
- IEEE Reconfigurable Architectures Workshop (RAW), Ranked B3: 2014, and 2015
- IEEE International Conference on Cyber, Physical and Social Computing (CPSCoM): 2015
- International Symposium on Applied Reconfigurable Computing (ARC): 2014
- HiPEAC Workshop on Reconfigurable Computing (WRC): 2014
- IEEE International Conference on Networking, Architecture, and Storage (NAS): 2013
- IEEE/IFIP International Conference on Embedded and Ubiquitous Computing (EUC), Ranked B1: 2012

2.2.4 Program Vice-Chair

- IEEE Reconfigurable Architectures Workshop (RAW), Ranked B3: 2013
- IEEE/IFIP International Conference on Embedded and Ubiquitous Computing (EUC) - Embedded Systems and Hardware/Software Co-Design, Ranked B1: 2011

2.2.5 Topic Chair

- Topic Chair for the topic A6: Reliable and Reconfigurable Systems in Design, Automation & Test in Europe (DATE), Ranked A1: 2015

2.2.6 Topic Co-Chair

- Topic Co-Chair for the topic A6: Reliable and Reconfigurable Systems in Design, Automation & Test in Europe (DATE), Ranked A1: 2012, 2013, and 2014

2.2.7 Track Chair

- ACM/SIGAPP Symposium On Applied Computing Embedded Systems Track: 2022, and 2023
- IEEE International Conference on Field Programmable Logic and Applications (FPL), Ranked A1: 2013, and 2021

2.2.8 Workshop Organizer

- IEEE Reconfigurable Architectures Workshop (RAW), Ranked B3: since 2016
- FPL Workshop on Reconfigurable Computing for Machine Learning: 2019, 2020, 2021, and 2022
- International Workshop on Computing in Heterogeneous, Autonomous 'N' Goal-oriented Environments (CHANGE): 2011, 2012, 2013, 2014, 2015, and 2016
- International Conference on Industrial and Information System: 2007

2.2.9 Program Committee

I've been involved in 35 conferences and 8 workshops as program committee members, among them:

- Design Automation Conference (DAC), Ranked A1: 2012, 2013, 2014, 2020, 2021, and 2022
- Design, Automation & Test in Europe (DATE), Ranked A1: 2012, 2013, 2014, 2015, 2016, 2019, 2020, 2021, and 2022
- International Conference on Computer-Aided Design (ICCAD), Ranked A1: 2015, 2016, 2017, 2019, and 2024
- IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM), Ranked A2: 2013, 2014, 2015, 2016, 2017, 2018, 2020, 2021, 2022, 2023, and 2024
- Conference on Hardware/Software CoDesign and System Synthesis (CODES-ISSS), Ranked A2: 2011, 2012, 2013, 2014, 2015, 2016, 2017, 2018, 2019, 2020, 2021 and 2022
- IEEE International Conference on Field Programmable Logic and Applications (FPL), Ranked A2: 2008, 2009, 2010, 2011, 2012, 2013, 2014, 2015, 2016, 2017, 2018, 2019, 2021, and 2022
- ACM International Conference on Supercomputing (ICS), Ranked A2: 2020, and 2022

2.3 Invited talks and Panelists

- **Invited talks**

- *The NECSTLab Multi-Faceted Experience with AWS F1 - Teaching, Research Framework and Application stack* - Keynote Speech
Speaker: M. D. Santambrogio
HiPEAC Workshop on Reconfigurable Computing (WRC), Valencia, Spain, 21 Jan, 2019.
- *Heterogeneous exascale Supercomputing: the Role of CAD in the exaFPGA Project.*
Speaker: M. D. Santambrogio.
Design, Automation & Test in Europa, Talk in a special session at DATE 17, Lausanne, Switzerland, 28 March, 2017
- *A self-adaptive approach to efficiently manage energy and performance in tomorrow's heterogeneous computing systems.*
Speaker: M. D. Santambrogio.
Design, Automation & Test in Europa, Talk in an special session at DATE 16, Dresden, Germany, 16 March, 2016
- *Operating System-Level Performance and Power Management: from Datacenters to Embedded Systems.*
Speaker: M. D. Santambrogio.
The International Conference on Hardware-Software Codesign and System Synthesis, CODES+ISSS 15, Amsterdam, Dutch, 6 October, 2015
- *The Autonomic Operating System Research Project - Achievements and Future Directions.*
Speaker: M. D. Santambrogio.
Design Automation Conference, DAC 2013, Austin, Texas, June 2 - 6, 2013
- *How to enable FPGA-based self-adaptive computing systems* - Keynote Speech
Speaker: M. D. Santambrogio
Workshop co-located with FPL 2013 entitled "Challenges of Embedded Robotics. Can FPGAs Overcome Them?", Porto, Portugal, 6 September, 2013.
- *From Reconfigurable Architectures to Self-Adaptive Autonomic Systems.* - Keynote Speech
Speaker: M. D. Santambrogio
International Workshop on Reconfigurable and Multicore Embedded System, August 29, 2009.
- Since 2013, I gave more than 30 talks describing the *NECSTCamp Project* and the *NECSTLab* at different venues, e.g. Northwestern University, University of Illinois at Chicago, Xilinx at San Jose, Intel at Santa Clara, Oracle Labs at Redwood Shores, Microsoft at Mountain View, at the Center to Support Excellence in Teaching of the Stanford University, at UC Berkeley, and at MIT;
- In 2012 and 2011, I gave 6 invited talk describing the *CHANGE Project* focusing on enabling technologies for self-aware adaptive computing systems, at different venues, e.g. IBM Research at Austin, Oracle at Belmont, Yahoo at Santa Clara.

- **Panelist**

- April 24 - 15, 2012, Goteborg, Sweden, HiPEAC Computing Systems Week April 2012, *Design and runtime management of reconfigurable systems*
- July 9 - 11, 2012, York, UK, 7th International Workshop on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC), *Maturity of high level synthesis tools - useful ore just another hype?*

3 TEACHING ACTIVITIES CARRIED OUT IN ITALIAN OR FOREIGN UNIVERSITIES OR BODIES

To summarise the main achievements in my teaching activities, I would like to highlight the following:

- Taught **5 editions** of the Advanced Computer Architecture course at the University of Illinois at Chicago;
- Designed and taught **5 Coursera MOOCs** in english, with more than **18K students** enrolled worldwide;
- Teaching Assistant of **2 courses, 5 editions** overall, taught in english at the Advanced Learning and Research Institute, master in Embedded Systems, Lugano, Switzerland;
- Taught **5 PhD courses** in english, **8 editions** overall, at Politecnico di Milano;
- Advisor of **25 PhD students** at Politecnico di Milano.

3.1 Courses with a primary responsibility

- University: University of Illinois at Chicago (Chicago, Illinois - USA):
 - Course: Advanced Computer Architecture (CS/ECE/MENG 466) - Graduate Course (taught in English)
Teacher: prof. M. D. Santambrogio
Academic Year: 17/18, 13/14, 11/12, 10/11, 09/10
- Coursera
 - Course: FPGA computing systems: Background knowledge and introductory materials
<https://www.coursera.org/learn/fpga-intro>
Teacher: prof. M. D. Santambrogio
16036 students enrolled
Graded: 4.6/5
Available online since: April 2018
 - Course: Developing FPGA-accelerated cloud applications with SDAccel: Theory
<https://www.coursera.org/learn/fpga-sdaccel-theory>
Teacher: prof. M. D. Santambrogio
4000 students enrolled
Graded: 4.7/5
Available online since: April 2019
 - Course: Developing FPGA-accelerated cloud applications with SDAccel: Practice
<https://www.coursera.org/learn/fpga-sdaccel-practice>
Teacher: prof. M. D. Santambrogio
2631 students enrolled
Graded: 4.4/5
Available online since: May 2019
 - Course: FPGA computing systems: A Bird's Eye View
<https://www.coursera.org/learn/fpga-computing-systems>
Teacher: prof. M. D. Santambrogio
2220 students enrolled
Graded: 4.5/5
Available online since: October 2022
 - Course: FPGA computing systems: Partial Dynamic Reconfiguration
<https://www.coursera.org/learn/copy-of-fpga-intro>
Teacher: prof. M. D. Santambrogio
Graded: n.a.
Available online since: Nov 2022
- University: Politecnico di Milano (Milano, Italy):

– PhD Course

- * Course: Advanced Topic on Reconfigurable FPGA-Based Systems Design
Teacher: prof. M. D. Santambrogio, prof. A. R. Miele
Academic Year: 18/19, 16/17
- * Course: Advanced Topics on Heterogeneous System Architectures: architectures, programming models and resource management
Teacher: prof. M. D. Santambrogio, prof. A. R. Miele
Academic Year: 20/21, 17/18
- * Course: FPGA-Based Systems Design
Teacher: prof. M. D. Santambrogio
Academic Year: 13/14
- * Course: Parallelism in Wonderland; are you ready to see how deep the rabbit hole goes?
Teachers: prof. M. D. Santambrogio, prof. S. Campanoni
Academic Year: 13/14
- * Course: From Reconfigurable Hardware to Self-Adaptive Computer Architectures
Teacher: prof. M. D. Santambrogio
Academic Year: 13/14, 12/13

– Master Degree

- * Course: Advanced Computer Architecture - Graduate Course
Teachers: prof. M. D. Santambrogio
Academic Year: 23/24, 22/23, 21/22, 20/21, 19/20
- * Course: High Performance and Processors and Systems - Graduate Course
Teachers: prof. M. D. Santambrogio
Academic Year: 23/24, 22/23, 21/22, 20/21, 19/20

– Undergraduate Course

- * Course: Fondamenti di Informatica - (Bio Eng students)
Teacher: prof. M. D. Santambrogio
Academic Year: 23/24, 22/23
- * Course: Informatica ed Elementi di Informatica Medica - (Bio Eng students)
Teacher: prof. M. D. Santambrogio
Academic Year: 21/22, 20/21, 19/20, 18/19, 17/18, 16/17, 15/16, 14/15, 13/14, 12/13, 11/12
- * Course: Informatica B - (Mech Eng studentes)
Teacher: prof. M. D. Santambrogio
Academic Year: 22/23, 21/22, 20/21, 19/20, 18/19, 17/18, 16/17, 15/16, 14/15, 13/14, 10/11
- * Course: Projects of Ingegneria Informatica - Undergraduate Course
Teacher: prof. M. D. Santambrogio
Academic Year: 09/10, 08/09

3.2 Teaching Assistantships

- University: Advanced Learning and Research Institute, master in Embedded Systems (Lugano, Switzerland):
 - Course: Design Technologies - Graduate course (taught in English)
Teacher: prof. G. De Micheli
Academic Year: 07/08, 06/07
 - Course: Validation and Verification - Graduate course (taught in English)
Teacher: prof. F. Somenzi
Academic Year: 06/07, 05/06, 04/05
- University: Politecnico di Milano (Milano, Italy):
 - Course: Architettura Avanzata dei Calcolatori (Advanced Computer Architecture) - Graduate Course
Teacher: prof. D. Sciuto
Academic Year: 18/19/ 17/18, 16/17, 15/16, 14/15, 10/11

- Course: High Performance and Processors and Systems - Graduate course (taught in English)
Teacher: prof. D. Sciuto
Academic Year: 18/19/ 17/18, 16/17, 15/16, 14/15, 13/14, 12/13, 11/12, 10/11, 09/10, 07/08, 06/07
- Course: Architettura Avanzata dei Calcolatori (Advanced Computer Architecture) - Graduate Course
Teacher: prof. R. Negrini
Academic Year: 12/13, 11/12
- Course: Architettura dei Calcolatori (Computer Architecture) - Graduate Course
Teacher: prof. D. Sciuto
Academic Year: 08/09, 07/08, 06/07
- Course: Reti Logiche A - Undergraduate Course
Teacher: prof. C. Bolchini
Academic Year: 08/09, 07/08, 06/07, 05/06, 04/05
- Course: Reti Logiche B - Undergraduate Course
Teacher: prof. F. Salice
Academic Year: 05/06
- Course: Informatica I - Undergraduate Course
Teacher: prof. C. Bolchini
Academic Year: 05/06
- University: Università degli Studi di Milano (Crema, Italy)
 - Course: Sistemi Operativi (Operating System) - Undergraduate Course
Teacher: prof. V. Piuri
Academic Year: 08/09, 07/08, 06/07, 05/06

3.3 PhD, MSc and Bachelor Theses Supervision

- 8 PhD Students, still enrolled in the program at Politecnico di Milano
- Advisor of 18 PhD Theses at Politecnico di Milano:
 - *Leveraging Heterogeneous Hardware Acceleration from High-level Programming Languages: The Case for Biomedical Informatics*
Student: G. W. Di Donato. Politecnico di Milano, Feb 2024;
 - *A Framework for the Aided Design of High-Performance Genome Analysis Applications on Heterogeneous Architectures*
Student: A. Zeni. Politecnico di Milano, Feb 2024;
 - *Data analytics for the nervous system activity: new feature extraction tools*
Student: L. Clementi. Politecnico di Milano, Feb 2024;
 - *On How to Optimize Medical Image Analysis: the Chimera Approach.*
Student: E. D'Arnese. Politecnico di Milano, Feb 2023;
 - *On how to facilitate hardware acceleration of machine learning for non-experts in hardware design over the Edge, the Fog, and the Cloud.*
Student: A. Damiani. Politecnico di Milano, Feb 2023;
 - *On the Role of Reconfigurable Systems in Domain-Specific Computing.*
Student: D. Conficconi. Politecnico di Milano, 17 Feb 2022;
 - *The Case for Reconfigurable Architectures in High-Performance Graph and Sparse Information Retrieval.*
Student: A.Parravicini. Politecnico di Milano, 17 Feb 2022;
 - *On the management of power and performance trade-offs in distributed cloud-native infrastructures.*
Student: R. Brondolin. Politecnico di Milano, 29 Oct. 2020;
 - *Hugenomic: Exploiting FPGAs as Hardware Accelerators in the Genomic Domain.*
Student: L. Di Tucci. Politecnico di Milano, 29 Oct. 2020;

- *Optimising Data-Intensive Applications for Modern Hardware Platforms.*
Student: A. Scolari. Politecnico di Milano, 6 Feb 2019;
 - *On How to Design Optimized Spatial Architectures: from Iterative Stencils to Convolutional Neural Networks.*
Student: G. Natale. Politecnico di Milano, 6 Feb 2019;
 - *CAOS: CAD as an Adaptive Open-platform Service for High Performance Reconfigurable Systems.*
Student: M. Rabozzi. Politecnico di Milano, 6 Feb 2019;
 - *On How to Effectively Target FPGAs from Domain Specific Tools.*
Student: E. Del Sozzo. Politecnico di Milano, 6 Feb 2019;
 - *Enabling power-awareness for multi-tenant systems.*
Student: M. Ferroni. Politecnico di Milano, 22 Feb 2017;
 - *On the design of autonomic techniques for runtime resource management in heterogeneous systems.*
Student: G. C. Durelli. Politecnico di Milano, 5 Feb 2016;
 - *On the role of polyhedral analysis in high performance reconfigurable hardware based computing systems.*
Student: R. Cattaneo. Politecnico di Milano, 17 Dec 2015;
 - *Techniques and Tools for Efficient, Qos-Driven Warehouse-Scale Computing.*
Student: D. B. Bartolini. Politecnico di Milano, 16 Feb 2015;
 - *System Support for Adaptive Performance and Thermal Management of Chip-Multiprocessors.*
Student: F. Sironi. Politecnico di Milano, 21 March 2014;
- **Advisor of the following Master Theses in CS at UIC, from 2008: 37**
 - **Advisor of the following Master Theses in BIOE at UIC, from 2018: 4**
 - **Advisor of Master Theses in Computer Engineering at Politecnico di Milano, from 2009: 81**
 - **Advisor of Master Theses in Biomedical Engineering at Politecnico di Milano, from 2016: 16**
 - **Advisor of Master Theses in Electronics Engineering at Politecnico di Milano, from 2018: 4**
 - **Advisor of Master Theses in Mathematical Engineering at Politecnico di Milano, from 2021: 2**
 - **Advisor of Master Theses in Automation and Control Engineering at Politecnico di Milano, from 2024: 1**

4 SCIENTIFIC RESPONSIBILITY FOR FUNDED RESEARCH PROJECTS AND AWARDS

To summarise the main achievements in this section, I would like to highlight the following:

- PI of **1** EU funded projects, and involved as work package/task leader in **2** other EU funded projects.
- PI of **9** private company funded projects for a total of **934K EUR** in income.

4.1 Research Grants

- **H2020 EXTRA European project.**
PoliMi PI: M. D. Santambrogio
Period: Sept 2015 - Sept 2018
Funding: 450K EUR
Santambrogio's role in EXTRA:
 - PoliMi PI for EXTRA
 - General Assembly Member of the EXTRA project
 - Work package Leader of WP4 (*Development of Reconfigurable Tools Platform*)
- **FP7 FASTER European project.**
PoliMi PI: Prof. D. Sciuto (donatella.sciuto@polimi.it)
Period: Sept 2011 - Dec 2014
Santambrogio's role in FASTER:
 - Work package Leader of WP2 (*High-level analysis and reconfigurable system definition*)
 - Task Leader of the following tasks: T2.2 (*Application task profiling and identification of reconfigurable cores*) and T2.4 (*Compile-time baseline scheduling and core mapping onto reconfigurable regions*)
- **FP7 SAVE European project.**
PoliMi PI: Prof. C. Bolchini (cristiana.bolchini@polimi.it)
Period: Sept 2013 - Sept 2016
Santambrogio's role in SAVE:
 - Task Leader of the following tasks: T3.1 (*Adaptive host OS components*) and T3.2 (*Adaptation policies/strategies*)
- **Fondazione Cariplo - Regione Lombardia**
Project Title: A Challenges Driven Design for Effective and Efficient Autonomic Mobile Computing Architectures.
Period: Oct 2016 - March 2018
Funding: 100K EUR
Santambrogio's role in the project: Principal Investigator
- **Huawei Technologies Switzerland AG**
Project Title: Templated Spatial Architectures.
Period: Sept 2021 - Dic 2022
Funding: 204K \$
Santambrogio's role in the project: Principal Investigator
- **Oracle Labs**
Project Title: Leveraging accelerators for efficient data processing in the cloud through GrCUDA enhancements and maintenance.
Period: Jun 2021 - June 2022
Funding: 150K \$
Santambrogio's role in the project: Principal Investigator

- **Oracle Labs**
 Project Title: Leveraging accelerators for efficient data processing in the cloud.
 Period: Feb 2020 - Feb 2021
 Funding: 100K \$
 Santambrogio's role in the project: Principal Investigator
- **Oracle Labs**
 Project Title: Enabling real-time accurate entity linking and other analytics on knowledge graphs.
 Period: June 2018 - June 2020
 Funding: 200K EUR (100K EUR per year)
 Santambrogio's role in the project: Principal Investigator
- **RSE S.p.A.**
 Project Title: Graphs analysis and graph machine learning applied to electrical networks.
 Period: Sept 2022 - Dec 2024
 Funding: 72K EUR
 Santambrogio's role in the project: Principal Investigator
- **RSE S.p.A.**
 Project Title: Enabling Complex Network Analysis in Multi-Energy Scenarios.
 Period: July 2020 - Dec 2021
 Funding: 45K EUR
 Santambrogio's role in the project: Principal Investigator
- **E-Novia**
 Project Title: Wearable ECG Monitoring System.
 Period: Jan 2020 - Dec 2020
 Funding: 50K EUR
 Santambrogio's role in the project: Principal Investigator
- **Polisocial Award 2022**
 Project Title: PReventive and ecologic Engineering Strategies for fragile bones: Towards green healthcare Objectives.
 Period: Oct 2022 - Oct 2023
 Funding: 100K \$
 Santambrogio's role in the project: Project Manager
- **Humanitas**
 Project Title: HUNA: Humanitas University NECST Application
 Period: Dec 2016 - Jun 2018
 Funding: 75K EUR
 Santambrogio's role in the project: Principal Investigator
- **MathWorks Academic Support**
 Project Title: Teaching Quantum Computing in MATLAB.
 Period: May 2014 - Dec 2014
 Funding: 30K EUR
 Santambrogio's role in the project: Principal Investigator
- **MathWorks Academic Support**
 Project Title: Teaching computer programming and embedded systems with audio processing in MATLAB.
 Period: Sept 2016 - Jun 2017
 Funding: 38K EUR
 Santambrogio's role in the project: Principal Investigator
- **Progetto Rocca Workshops and Colloquia.**
 Collaboration between the MIT-CARBON Group and Politecnico di Milano - DRESO Group.
 Period: January 2010
 Funding: 25K USD

- **Swiss NSF Research Project (Division II).**
Project title: *Dynamically Adaptive Architectures for Nomadic Embedded Systems*.
Period: 02/2010 - 01/2013.
Partners: EPFL, Prof. David Atienza, in cooperation with Politecnico di Milano (IT); Prof. Donatella Sciuto and Dr. Marco D. Santambrogio.
- **HiPEAC Collaboration Grant.**
Title of the research: Self-Aware Reconfigurable Computing Systems for Energy Saving and Performance Enhancement.
Period: November 2010 - December 2011
Funding: 5K EUR
- **HiPEAC Collaboration Grant.**
Title of the research: Self-aware and autonomic system.
Period: July 2009
Funding: 5K EUR

4.2 Awards

- Paper winner of the **BHI 2019 Best Paper Award**. (*"circFA: a FPGA-based circular RNA aligner"*. [<https://ieeexplore.ieee.org/document/8834539>])
- Paper winner of the **EWiLi 2013 Best Paper Award**. (*"A Performance-Aware Quality of Service-Driven Scheduler for Multicore Processors"*. [[28]])
- **Best Student Paper award sponsored by IEEE TCPP: 7th IEEE International Conference on Autonomic Computing (ICAC) 2010** (*Smartlocks: Lock Acquisition Scheduling for Self-Aware Synchronization* [[129]])
- Best Paper Award Finalist, IEEE International Conference on Field Programmable Logic and Applications (FPL) 2009 (*A Runtime Relocation Based Workflow for Self Dynamic Reconfigurable Systems Design* [[145]])
- **Best paper award: 15th International Conference on Very Large Scale Integration, IFIP VLSI-SoC 2007** (*ReCPU: a Parallel and Pipelined Architecture for Regular Expression Matching* [[169]])
- Paper winner of the **2012 HiPEAC Paper Award**. (*"Metronome: Operating System Level Performance Management via Self-Adaptive Computing"*. [[121]])
- Paper winner of the **RAW 2016 Best Demo Award**. (*"On the Automation of High Level Synthesis of Convolutional Neural Networks"*. [[31]])
- Advisor of the PYNQ category winners of the **Xilinx Open Hardware Contest 2022**. (PYNQ Category winner *"A Journey to the center of the 3D Space"*, [<https://www.openhw.eu/2022-results-gallery>])
- Advisor of the PhD category winners of the **Xilinx Open Hardware Contest 2020**. (PhD Category winner *"Personalized PageRank low-latency Recommender Systems"*, [<http://www.openhw.eu/2020-results.html>])
- Advisor of the AWS EC2 F1 category winners of the **Xilinx Open Hardware Contest 2018**. (AWS EC2 F1 Category winner *"5 Points to Rule Them All"*, [<http://www.openhw.eu/2018-finalists.html>])
- Advisor of the PhD category winners of the **Xilinx Open Hardware Contest 2017**. (PhD Category winner *"bibbidi N-BObbiDY boo: Magic Acceleration of N-Body Simulation"*, [www.openhw.eu/2017-finalists.html])
- Advisor of the PhD and Student FPGA category winners of the **Xilinx Open Hardware Contest 2016**. (PhD Category winner *"exaFPGA: Iterative stencil cell loop acceleration"*; Student FPGA Category winner *ProFAX: Protein folding on FPGA* [www.openhw.eu/2016-finalists.html])
- December, 2008. awarded a **Progetto Rocca Postdoc Fellowship at MIT**.

- **Dimitri N. Chorafas PhD Thesis Award** from the Chorafas Foundation (Berne, Switzerland) for the best PhD Theses in "Systems Engineering and Information Technology", May 2008. Thesis title: *Hardware/Software codesign methodologies for dynamically reconfigurable systems*)

5 TECHNOLOGY TRANSFER

To summarise the main achievements with respect to the technology transfer, I would like to highlight the following:

- Founder of **2** startups, and a **third** one under constitution
- Creator of **7** patents

5.1 Startups and Spin-Offs

- **GenoGra**

Company name: GenoGra

Company website: <https://genogra.com/>

Founded: June 8, 2023

Santambrogio's role in GenoGra: Scientific Advisor

Award: Winner of the Switch2Product Innovation Challenge 2021, LifeScience & MedTech track, Dec 2021, 30K EUR

Semifinalist of the Stage Two Startup Competition 2022, GenoGra was selected to represent the Politecnico di Milano at the competition, Oct 2022

Award: Winner of the StartCup Lombardia 2022, LifeScience & MedTech track, Oct 27, 2022, 25K EUR

- **Huxelerate**

Company name: Huxelerate S.R.L.

Company website: <https://www.huxelerate.it/>

Founded: Feb 2, 2019

Revenue: 2020 ~20K EUR, 2021 ~112K EUR

Santambrogio's role in Huxelerate: Co-Founder & Scientific Advisor

Co-Founders: Lorenzo Di Tucci, Sara Notargiacomo, Marco Rabozzi, Marco Santambrogio

- **Arox**

Company name: Arox S.R.L.

Company website: <https://arox.io/>

Founded: November 28, 2018

Revenue: 2020 ~292K EUR, 2021 ~375K EUR, 2022 ~500K EUR

Santambrogio's role in Huxelerate: Co-Founder & Scientific Advisor

Co-Founders: Niccoló Consolazio, Sara Notargiacomo, Luca Paccani, Marco Santambrogio, Davide Toschi

5.2 Patents

- **ID: 102022000004439**

Title: Method for the alignment of sequence reads to cyclic genome graphs on heterogeneous computing systems

Assignee: Politecnico Di Milano

Inventor/Author: Guido Walter Di Donato, Alberto Zeni, Mirko Coggi, Guglielmo Bruno and MARCO D. SANTAMBROGIO

Priority date: 09/03/2022

Filing/creation date: 09/03/2022

Publication date: class G16B20, European Patent Office. Pending

Result link: N/A (the patent is still in the secrecy period)

- **ID: 102021000021125**

Title: Dispositivo diagnostico indossabile

Assignee: Politecnico di Milano, e-Novia

Inventor/Author: Davide Bruschi, Luca Testa, Nicola Giuseppe Trapletti, Glauco Bigini, Eleonora D'Arnese, Letizia Clementi, MARCO D. SANTAMBROGIO

Priority date: 04/08/2021

Filing/creation date: 04/08/2021

Publication date: Pending

Result link: N/A (the patent is still in the secrecy period)

- **ID: US-2019102233-A1**
 Title: Method for power optimization in virtualized environments and system implementing the same
 Assignee: Politecnico Di Milano
 Inventor/Author: MARCO D. SANTAMBROGIO, Matteo Ferroni, Marco Arnaboldi
 Priority date: 2017-10-04
 Filing/creation date: 2017-10-04
 Publication date: 2019-04-04
 Result link: <https://patents.google.com/patent/US20190102233A1/en>
- **ID: WO-2020217200-A1**
 Title: Method of aligning strings of characters representing genomic data and related hardware device
 Assignee: Huxelerate S.R.L.
 Inventor/Author: Alberto Zeni, Matteo Crespi, Lorenzo Di Tucci, MARCO D. SANTAMBROGIO, Fabio Pizzato
 Priority date: 2019-04-23
 Filing/creation date: 2020-04-23
 Publication date: 2020-10-29
 Result link: <https://patents.google.com/patent/WO2020217200A1/en>
- **ID: WO-2019116213-A1**
 Title: Method for locating a device inside an area
 Assignee: Politecnico Di Milano
 Inventor/Author: Donatella Sciuto, MARCO D. SANTAMBROGIO, Alessandro Antonio Nacci, Alessandro Frossi, Niccoló Consolazio, Luca Paccani, Andrea Cirigliano
 Priority date: 2017-12-11
 Filing/creation date: 2018-12-11
 Publication date: 2019-06-20
 Result link: <https://patents.google.com/patent/WO2019116213A1/en>
- **ID: WO-2020234792-A1**
 Title: Système fpga-as-a-service pour informatique sans serveur accélérée
 Assignee: Politecnico Di Milano
 Inventor/Author: MARCO D. SANTAMBROGIO, Rolando Brondolin, Marco Bacis
 Priority date: 2019-05-21
 Filing/creation date: 2020-05-20
 Publication date: 2020-11-26
 Result link: <https://patents.google.com/patent/WO2020234792A1/fr>
- **ID: WO-2020217201-A1**
 Title: Procédé de réalisation d'un dispositif matériel pour exécuter des opérations définies par un code logiciel de haut niveau
 Assignee: Huxelerate S.R.L.
 Inventor/Author: Marco Siracusa, Marco Rabozzi, Lorenzo Di Tucci, MARCO D. SANTAMBROGIO, Fabio Pizzato
 Priority date: 2019-04-26
 Filing/creation date: 2020-04-23
 Publication date: 2020-10-29
 Result link: <https://patents.google.com/patent/WO2020217201A1/fr>

6 PUBLICATIONS

6.1 Productivity and Impact Metrics

- Scientific Productivity: 300+ publications (339 entries on Scopus, 503 co-authors according to Scopus):
- Author/Co-author of **15 top-ranked Q1 journal papers**: [1, 2, 3, 4, 5, 6, 8, 19, 26, 29, 30, 34, 37, 40, 41] (including IEEE Transactions on Parallel and Distributed Systems, IEEE Transactions on Emerging Topics in Computing, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, IEEE Micro, ACM Transactions on Autonomous and Adaptive Systems, IEEE Transactions on Control Systems Technology, and ACM Computing Surveys (CSUR) from SCIMAGO ([HTTP://SCIMAGOJR.COM](http://scimagojr.com)))
- Author/Co-author of 250+ scientific publications on peer-reviewed conferences including 57 top-level A1/A2 Class 1 conferences (ASP-DAC, CODESS+ISSS, DAC, DATE, FCCM, FPGA, FPL, ICAC, ICCAD, IPDPS, ISCAS, OSDI, PACT, PPOPP, UbiComp) from Conference Ranks ([HTTP://WWW.CONFERENCERANKS.COM/#DATA](http://www.conferenceranks.com/#DATA)).
- Publication Impact:
 - Based on Google Scholar: h-index 41, citations 6025
 - Based on Scopus: h-index 28, citations 3322
 - Based on SciVal: h-index 28

6.2 List of all the publications

Book

- [1] Pao-Ann Hsiung, M. D. SANTAMBROGIO, and Chun-Hsian Huang. *Reconfigurable System Design and Verification*. Taylor & Francis/CRC Press, 2009.

Journals

- [1] Davide Conficconi, Emanuele Del Sozzo, Filippo Carloni, Alessandro Comodi, Alberto Scolari, and MARCO DOMENICO SANTAMBROGIO. “An energy-efficient domain-specific architecture for regular expressions”. In: *IEEE Transactions on Emerging Topics in Computing* (2022).
- [2] Davide Conficconi, Eleonora D’Arnese, Emanuele Del Sozzo, Luigi Fusco, Donatella Sciuto, and MARCO DOMENICO SANTAMBROGIO. “Faber: a Hardware/Software Toolchain for Image Registration”. In: *IEEE Transactions on Parallel and Distributed Systems (TPDS)* (2022).
- [3] Andrea Damiani, Giorgia Fiscaletti, Marco Bacis, Rolando Brondolin, and Marco D. Santambrogio. “BlastFunction: A Full-Stack Framework Bringing FPGA Hardware Acceleration to Cloud-Native Applications”. In: *ACM Trans. Reconfigurable Technol. Syst.* 15.2 (2022). ISSN: 1936-7406. DOI: 10.1145/3472958. URL: <https://doi.org/10.1145/3472958>.
- [4] Eleonora D’Arnese, Guido Walter Di Donato, Emanuele Del Sozzo, Martina Sollini, Donatella Sciuto, and MARCO DOMENICO SANTAMBROGIO. “On the automation of radiomics-based identification and characterization of nscl”. In: *IEEE Journal of Biomedical and Health Informatics* 26.6 (2022), pp. 2670–2679.
- [5] Emanuele Del Sozzo, Davide Conficconi, Alberto Zeni, Mirko Salaris, Donatella Sciuto, and MARCO DOMENICO SANTAMBROGIO. “Pushing the Level of Abstraction of Digital System Design: a Survey on How to Program FPGAs”. In: *ACM Computing Surveys (CSUR)* (2022).

- [6] Marco Siracusa, Emanuele Del Sozzo, Marco Rabozzi, Lorenzo Di Tucci, Samuel Williams, Donatella Sciuto, and MARCO DOMENICO SANTAMBROGIO. “A Comprehensive Methodology to Optimize FPGA Designs via the Roofline Model”. In: *IEEE Transactions on Computers* 71.8 (2022), pp. 1903–1915. DOI: 10.1109/TC.2021.3111761.
- [7] Daniele Parravicini, Davide Conficconi, Emanuele Del Sozzo, Christian Pilato, and Marco D Santambrogio. “CICERO: A Domain-Specific Architecture for Efficient Regular Expression Matching”. In: *ACM Transactions on Embedded Computing Systems (TECS)* 20.5s (2021), pp. 1–24.
- [8] Enrico Reggiani, Emanuele Del Sozzo, Davide Conficconi, Giuseppe Natale, Carlo Moroni, and Marco D Santambrogio. “Enhancing the scalability of multi-fpga stencil computations via highly optimized hdl components”. In: *ACM Transactions on Reconfigurable Technology and Systems (TRETs)* 14.3 (2021), pp. 1–33.
- [9] Samuele Barbieri, Fabiola Casasopra, Rolando Brondolin, and MARCO DOMENICO SANTAMBROGIO. “FARD: accelerating distributed fog computing workloads through embedded FPGAs”. In: *ACM SIGBED Review* 17.1 (2020), pp. 56–62.
- [10] Rolando Brondolin, Marco Arnaboldi, and MARCO DOMENICO SANTAMBROGIO. “Power consumption management under a low-level performance constraint in the Xen hypervisor”. In: *ACM SIGBED Review* 17.1 (2020), pp. 42–48.
- [11] Rolando Brondolin and MARCO DOMENICO SANTAMBROGIO. “A Black-box Monitoring Approach to Measure Microservices Runtime Performance”. In: *ACM Transactions on Architecture and Code Optimization (TACO)* 17.4 (2020), pp. 1–26.
- [12] Luca Cerina and MARCO DOMENICO SANTAMBROGIO. “SAGE: a configurable code generator for efficient symbolic analysis of time-series”. In: *ACM SIGBED Review* 17.1 (2020), pp. 12–17.
- [13] Luca Cerina, MARCO DOMENICO SANTAMBROGIO, Giuseppe Franco, Claudio Gallicchio, and Alessio Micheli. “EchoBay: Design and optimization of echo state networks under memory and time constraints”. In: *ACM Transactions on Architecture and Code Optimization (TACO)* 17.3 (2020), pp. 1–24.
- [14] Luca Stornaiuolo, Filippo Carloni, Riccardo Pressiani, Giuseppe Natale, MARCO DOMENICO SANTAMBROGIO, and Donatella Sciuto. “Enabling transparent hardware acceleration on Zynq SoC for scientific computing”. In: *ACM SIGBED Review* 17.1 (2020), pp. 30–35.
- [15] F Barbic, M Minonzio, B Cairo, D Shiffer, A Dipasquale, L Cerina, A Vatteroni, V Urechie, P Verzeletti, F Badilini, et al. “Effects of different classroom temperatures on cardiac autonomic control and cognitive performances in undergraduate students”. In: *Physiological measurement* 40.5 (2019), p. 054005.
- [16] Rolando Brondolin, Matteo Ferroni, and MARCO DOMENICO SANTAMBROGIO. “Performance - aware load shedding for monitoring events in container based environments”. In: *ACM SIGBED Review* 16.3 (2019), pp. 27–32.
- [17] Cristiana Bolchini, Stefano Cherubin, Gianluca C Durelli, Simone Libutti, Antonio Miele, and MARCO DOMENICO SANTAMBROGIO. “A runtime controller for OpenCL applications on heterogeneous system architectures”. In: *ACM SIGBED Review* 15.1 (2018), pp. 29–35.
- [18] Matteo Ferroni, Juan A Colmenares, Steven Hofmeyr, John D Kubiawicz, and MARCO DOMENICO SANTAMBROGIO. “Enabling power-awareness for the xen hypervisor”. In: *ACM SIGBED Review* 15.1 (2018), pp. 36–42.
- [19] Matteo Ferroni, Andrea Corna, Andrea Damiani, Rolando Brondolin, John D Kubiawicz, Donatella Sciuto, and Marco D Santambrogio. “MARC: a resource consumption modeling service for self-aware autonomous agents”. In: *ACM Transactions on Autonomous and Adaptive Systems (TAAS)* 12.4 (2017), pp. 1–29.
- [20] M. Rabozzi, G. C. Durelli, A. Miele, J. Lillis, and MARCO DOMENICO SANTAMBROGIO. “Floorplanning Automation for Partial-Reconfigurable FPGAs via Feasible Placements Generation”. In: *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)* 25.1 (2017), pp. 151–164. ISSN: 1063-8210. DOI: 10.1109/TVLSI.2016.2562361.

- [21] Riccardo Cattaneo, Giuseppe Natale, Carlo Sicignano, Donatella Sciuto, and MARCO DOMENICO SANTAMBROGIO. “On How to Accelerate Iterative Stencil Loops: A Scalable Streaming-Based Approach”. In: *ACM Transactions on Architecture and Code Optimization (TACO)* 12.4 (2016), p. 53. DOI: 10.1145/2842615. URL: <http://doi.acm.org/10.1145/2842615>.
- [22] Gianluca C. Durelli and MARCO DOMENICO SANTAMBROGIO. “Autonomic thread scaling library for QoS management”. In: *SIGBED Review* 13.1 (2016), pp. 41–47. DOI: 10.1145/2907972.2907978. URL: <http://doi.acm.org/10.1145/2907972.2907978>.
- [23] Alberto Scolari, Davide Basilio Bartolini, and MARCO DOMENICO SANTAMBROGIO. “A Software Cache Partitioning System for Hash-Based Caches”. In: *ACM Transactions on Architecture and Code Optimization (TACO)* 13.4 (Dec. 2016), 57:1–57:24. ISSN: 1544-3566. DOI: 10.1145/3018113. URL: <http://doi.acm.org/10.1145/3018113>.
- [24] Dionisios N. Pnevmatikatos, Kyprianos Papadimitriou, Tobias Becker, Peter Böhm, Andreas Brokalakis, Karel Bruneel, C. Ciobanu, Tom Davidson, Georgi Gaydadjiev, Karel Heyse, Wayne Luk, Xinyu Niu, Ioannis Papaefstathiou, Danilo Pau, Oliver Pell, Christian Pilato, MARCO DOMENICO SANTAMBROGIO, Donatella Sciuto, Dirk Stroobandt, Tod Todman, and Elias Vansteenkiste. “FASTER: Facilitating Analysis and Synthesis Technologies for Effective Reconfiguration”. In: *Microprocessors and Microsystems - Embedded Hardware Design* 39.4-5 (2015), pp. 321–338. DOI: 10.1016/j.micpro.2014.09.006. URL: <http://dx.doi.org/10.1016/j.micpro.2014.09.006>.
- [25] Davide B. Bartolini, Filippo Sironi, Donatella Sciuto, and MARCO DOMENICO SANTAMBROGIO. “Automated Fine-Grained CPU Provisioning for Virtual Machines”. In: *ACM Transactions on Architecture and Code Optimization (TACO)* 11.3 (2014), 27:1–27:25. DOI: 10.1145/2637480. URL: <http://doi.acm.org/10.1145/2637480>.
- [26] Xabier Iturbe, Ali Ebrahim, Khaled Benkrid, Chuan Hong, Tughrul Arslan, Jon Perez, Didier Keymeulen, and MARCO DOMENICO SANTAMBROGIO. “R3TOS-Based Autonomous Fault-Tolerant Systems”. In: *IEEE Micro* 34.6 (2014), pp. 20–30. DOI: 10.1109/MM.2014.58. URL: <http://dx.doi.org/10.1109/MM.2014.58>.
- [27] Jacopo Panerati, Martina Maggio, Matteo Carminati, Filippo Sironi, Marco Triverio, and MARCO DOMENICO SANTAMBROGIO. “Coordination of Independent Loops in Self-Adaptive Systems”. In: *ACM Transaction on Reconfigurable Technology and Systems (TRETs)* 7.2 (2014), 12:1–12:16. DOI: 10.1145/2611563. URL: <http://doi.acm.org/10.1145/2611563>.
- [28] Filippo Sironi, Donatella Sciuto, and MARCO DOMENICO SANTAMBROGIO. “A performance-aware quality of service-driven scheduler for multicore processors”. In: *SIGBED Review* 11.1 (2014), pp. 50–55. DOI: 10.1145/2597457.2597464. URL: <http://doi.acm.org/10.1145/2597457.2597464>.
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